

Power and Temperature Prediction for Computer System Power Optimization

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Abstract

This paper investigates desktop computer system power optimization with Modelica. Firstly, microprocessor power equation is modeled with voltage and temperature dependency. Secondly, steady state heat transfer path is modeled as a variable thermal resistance with fan power change and is connected to microprocessor power model to discuss optimum working point of fan which minimizes power consumption of the power rail for the microprocessor on the target computer system under CPU-intensive workload condition. After that, transient heat transfer path modeling is explored as a Cauer thermal network creation.

Keywords: *Computer system, Microprocessor, Power Optimization*

1 Introduction

Computer systems are vital in the modern world. Higher performance is still explored not only for high performance computing systems and server systems but also for consumer computer systems such as desktop computers, notebook computers and slate devices. Also, IoT (Internet of Things) and M2M (Machine-to-Machine) infrastructure has been rapidly developed in a few years and computer systems for these use will be increased rapidly. While, energy consumption needs to be eliminated in the sustainable development of modern society and power consumption by computer systems is one of important subject to be solved.

The latest microprocessors incorporate power management features which control trade-off of computing performance and power consumption. With these features, microprocessor's power efficiency has been improved drastically in the past decade, however, system level power optimization is still on the way because system level power optimization needs to consider power consumption of not only microprocessor itself but also peripherals and power supply circuit for them. And power consumption of the microprocessor is highly dependent on temperature, however, current system-level temperature control methodology is to maintain junction temperature of microprocessor within operational temperature range and not to minimize

system-level power consumption.

To minimize system-level power consumption, power modeling methodology with practical accuracy is required. There are many efforts and researches on electrical characteristics on CMOS (Complementary Metal-Oxide-Semiconductor) circuits. And microprocessors incorporate power management features, while system-level power optimization is still on the way. Thus, author investigates microprocessor power equation to conduct both power and thermal control as a part of previous study (Nishi, 2012). In the study, microprocessor power equation with voltage and temperature dependencies is introduced and is employed in three-dimensional heat conduction simulation. However, three-dimensional simulation costs too much from a computational load standpoint and takes time to create accurate thermal simulation model. To enable fast simulation environment, three-dimensional simulation needs to be replaced by another methodology which ensures high speed calculation with practical accuracy. Also, model creation effort should be minimized as much as possible.

As another methodology to conduct thermal simulation with reduced computational load, there are thermal network methodology and model order reduction (MOR). Thermal network methodology has long history for temperature prediction. As for thermal network application to semiconductor devices, there already exist some researches in 1980s. For example, thermal network is utilized for temperature prediction of multi-chip module (Ishizuka and Fukuoka, 1986). Traditional way to create thermal network is to determine thermal resistance and heat capacitance values from dimensions and thermophysical properties of each component along heat transfer paths. In recent years, curve fitting technique to determine thermal resistance and heat capacitance values from measurement data is also sometimes employed. On the other hand, MOR is a technique to reduce computational complexity of simulation model and is sometimes utilized with Modelica. For example, MOR is applied to FEM (Finite Element Method) model and reduced order model is implemented as FMU (Functional Mockup Unit) (Gödecke *et al.*, 2012). Also, MOR based technique is proposed for thermal simulation as well (Codecasa *et al.*, 2014). MOR is useful if three-dimensional simulation model or dimensions and

thermophysical properties of each component along heat transfer paths are available.

This research aims to establish fast simulation environment for computer system power optimization with Modelica. In this paper, power equation is modeled as a Modelica component. Secondly, steady state heat transfer path is modeled as a Modelica component with a variable thermal resistance which expresses fan speed change of heat sink fan over the microprocessor. Thirdly, they are connected each other, and system-level power optimization is investigated. After that, transient heat transfer path modeling is explored as a Cauer thermal network creation, to establish transient control optimization environment.

2 Target Desktop Computer System

2.1 Hardware Configuration

The target computer system in this paper is a desktop personal computer, Sycom Radiant GZ2650X470A (Fig. 1 (a)). It employs a AMD Ryzen 5 1500X processor, which is fabricated with 14nm process technology and has 4 CPU cores with totally 8-thread execution capability. Its thermal design power (TDP) is 65 W. The base frequency of the microprocessor is 3.5 GHz, however, the microprocessor supports boosted frequency up to 3.7 GHz. Under lower temperature conditions, it runs over 3.5GHz with higher power consumption than TDP. Thus, a large heat sink fan prepared by microprocessor manufacturer is attached over the microprocessor package (Fig. 1 (b)). Table 1 shows major hardware components of the target computer system. The microprocessor consumes more than half of the computer system's power under CPU-intensive workload scenario and this paper focuses on microprocessor power.

2.2 Key Software Components

Key software components of the target computer system are listed in Table 2. The system is based on Ubuntu



Figure 1. Desktop personal computer outlook and heat sink fan for microprocessor.

16.04 (64-bit). Prime 95 is an application software and is utilized as a CPU-intensive workload in this paper. It processes FFT (Fast Fourier Transformation) continuously. Prime 95 has some test modes and “small FFT” is utilized in this paper. AMD μ Prof is utilized as a monitoring software tool which can log CPU temperature, estimated power consumption and so on.

3 Power Modeling

3.1 Microprocessor Power Equation

3.1.1 Power Equation of CMOS digital circuits

Power consumption of CMOS digital circuits, including the latest microprocessor, is due to electrical charge and discharge to/from load capacitance C_{load} and power loss by leakage current (Hiramoto *et al.*, 2009). Therefore, its power consumption can be modeled as the equation below (Kunimine *et al.*, 2011):

$$P_{CMOS} = aC_{load}V_{DD}^2f_{op} + I_{leak}V_{DD} \quad (1)$$

Here, a is activation rate, C_{load} is load capacitance, V_{DD} is power supply voltage, f_{op} is operational frequency and I_{leak} is leakage current. Unfortunately, it is known that C_{load} has voltage dependency (Uchida *et al.*, 2001; Uchida *et al.*, 2002; Watanabe *et al.*, 2007). Also, there are several types of leakage current (Hiramoto *et al.*,

Table 1. Major hardware components of target desktop computer system.

Function	Component
Microprocessor	AMD Ryzen 5 1500X (65W TDP)
Motherboard	MSI B350 TOMAHAWK
Memory	DDR4-2400 (16GB \times 2)
Graphics card	NVIDIA GeForce GT710 (1GB)
HDD	Toshiba DT01ACA100 (1TB)
Power supply	Antec NeoECO NE650C (650W)

Table 2. Major software components of target desktop computer system.

Function	Component
Operating system	Ubuntu 16.04 (64-bit)
Software utilized as CPU workload	Prime 95 v29.5 (Linux version 64-bit)
Processor information gathering	AMD μ Prof v1.2.275.0 (Linux version 64-bit)

2009). Many of them have voltage dependency. Moreover, subthreshold current, which is a dominant factor of leakage current has not only voltage dependency but also temperature dependency.

3.1.2 CPU Core Power Equation

For microprocessor CPU cores, V_{DD} needs to be changed when f_{op} is changed to increase computational performance or lower power consumption. Thus, C_{load} is changed when f_{op} is changed. Author investigated the way to express C_{load} for microprocessor silicon die temperature prediction and concluded linear approximation of V_{DD} works well because V_{DD} range of CPU core is not so much large during normal operation as a part of previous study (Nishi, 2012). As for leakage current, subthreshold current is modeled as exponential function of temperature for precise discussion (Amelifard, 2008). However, exponential function is not suitable for high speed electro-thermal simulation, especially for transient simulation, from a computational load standpoint. Also, microprocessor is utilized under temperature range from room ambient to around 100 deg C and it is relatively small range compared to other semiconductor devices such as power semiconductor. Thus, Author investigated the way to express leakage current for microprocessor silicon die temperature prediction and concluded linear approximation of V_{DD} and quadratic approximation of silicon die temperature T work well as a part of previous study (Nishi, 2012). Therefore, power consumption of a CPU core can be expressed as the equation below:

$$P_{CPU} = (d_1 V_{DD} + d_2) V_{DD}^2 f_{op} + (s_1 V_{DD} + s_2)(T^2 + s_3 T + s_4) V_{DD} \quad (2)$$

Here, d_1, d_2 are coefficients of the first term, called as dynamic power term, and s_1 to s_4 are coefficients of the second term, called as static power term, on the right in eq. (2).

3.1.3 Microprocessor Power Equation

Microprocessor has several power rails and sum of their power consumption equals to microprocessor power consumption. Since this paper focuses on CPU intensive workload case only and microprocessor power consumption other than CPU cores is relatively small and can be modeled as constant. Therefore, microprocessor power consumption in the case that all CPU cores run the same workload is

$$P_{Microprocessor} = n P_{CPU} + P_{Other} \quad (3)$$

Here, n is number of CPU cores and P_{Other} is power consumption by circuits other than CPU cores in microprocessor silicon die. Applying junction temperature T_j , which is reported as Die SoC temperature in AMD μ Prof, as silicon die temperature for P_{CPU} and assuming P_{Other} is constant, the

microprocessor power equation is obtained finally from eq. (2) and (3),

$$P_{Microprocessor} = (c_1 V_{DD} + c_2) V_{DD}^2 f_{op} + (c_3 V_{DD} + c_4)(T_j^2 + c_5 T_j + c_6) V_{DD} + c_7 \quad (4)$$

Here, c_1 to c_7 are coefficients of microprocessor power consumption. By determining these coefficients, microprocessor power consumption can be calculated.

3.2 Power Consumption of Microprocessor Power Rail

On the latest desktop computer system, EPS12V power rail works as microprocessor dedicated power supply rail from power supply unit to motherboard (Fig. 2). Since EPS12V has power loss by voltage regulators which convert 12V voltage level to several lower voltage levels for the microprocessor, EPS12V is thought as the key power rail for the target desktop computer system under CPU-intensive workload. Thus, not only microprocessor power but also EPS12V power are collected and modeled in this paper. Since EPS12V power is sum of microprocessor power and power loss of DC-DC conversion by voltage regulators of microprocessor power rails, it should take the same form as eq. (4) with different coefficient values from microprocessor.

3.3 Power Modeling of The Target Desktop Computer System

Microprocessor and EPS12V power are sensitive to application workload and usual application software changes activation rate in eq. (1) and eq. (2) dynamically. To collect consistent and accurate voltage and

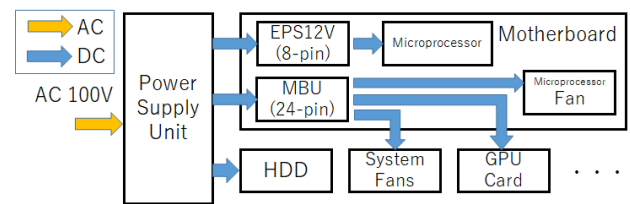


Figure 2. Power supply structure of target desktop computer system.

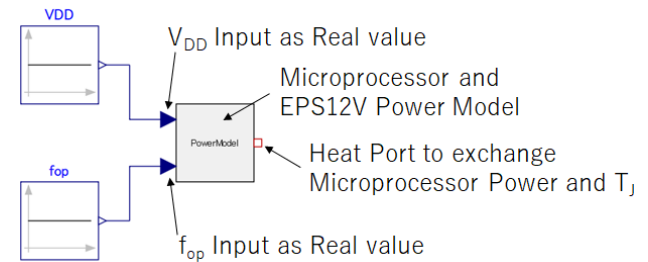


Figure 3. Microprocessor and EPS12V power model with V_{DD} and f_{op} inputs.

temperature dependent power data, constant workload should be added. In this paper, M172031, one of small FFT execution in "Torture Test" of Prime 95, is utilized and is added to all CPU threads. Totally eight M172031 modules run on target desktop computer system during measurement.

AMD μ Prof tool is utilized to read junction temperature and estimated microprocessor power. EPS12V power rail current and voltage are measured by current probe and data logger, respectively.

OpenModelica v1.13.2 is utilized to create Modelica models and conduct simulation in this paper. Figure 3 shows a created Modelica component model which calculates microprocessor and EPS12V power and T_J . Coefficients are obtained as parameters and only V_{DD} and f_{op} are externally obtained via connectors. A heat port is prepared to exchange microprocessor power and T_J with external component. Two Eq. (4), one for microprocessor and another for EPS12V, are expressed as Modelica equations. Figure 4 shows Modelica simulation result in the case that an ambient temperature component is connected to heat port of the power model and ambient temperature value is swept from 40 deg C to 70 deg C.

4 Heat Transfer Path Modeling

To obtain power consumption under real environment, junction temperature also needs to be calculated. Thus, heat transfer path is modeled as the thermal resistance from junction to ambient, $R_{th, JA}$, which can be utilized in steady state simulation (Nishi *et al*, 2019).

$$R_{th, JA} = \frac{T_J - T_A}{P_{Microprocessor}} \quad (5)$$

Here, T_A is ambient temperature.

Measurement is conducted with the same condition described in section 3.3 and thermal resistance is modeled as a function of fan power.

Figure 5 shows a created Modelica component model which calculates $R_{th, JA}$ from fan power input value. At this time, $R_{th, JA}$ is modeled as polynomial which is obtained by curve fitting of measurement result. Figure 6 shows thermal resistance variation by fan power.

5 Power Optimization Under Steady State

To obtain both microprocessor power and junction temperature, the equation below needs to be solved:

$$T_J = R_{th, JA} \cdot P_{Microprocessor} + T_A \quad (6)$$

In Modelica, eq. (6) is solved by connecting created Modelica component models in Fig. 3 and Fig. 5 as shown in Fig. 7.

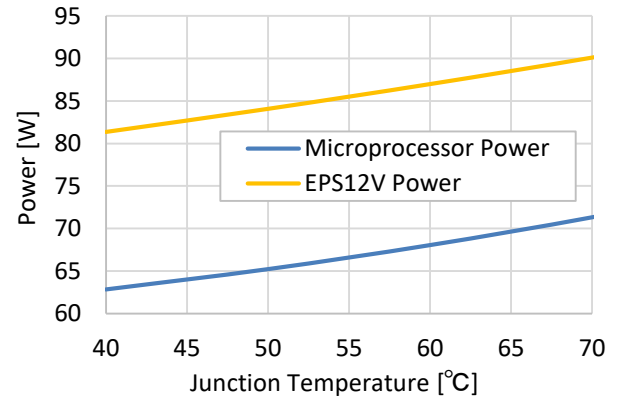


Figure 4. Relationship between junction temperature and power consumption.

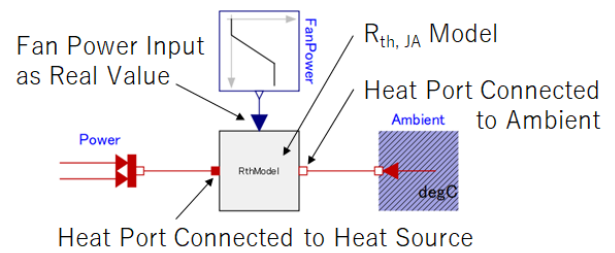


Figure 5. Thermal resistance model with fan power input and connections with heat source and ambient.

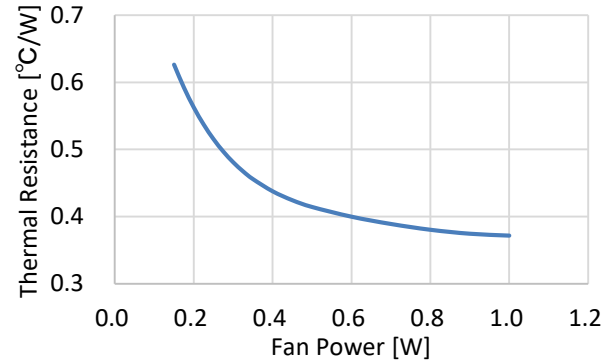


Figure 6. Relationship between fan power and thermal resistance from junction to ambient.

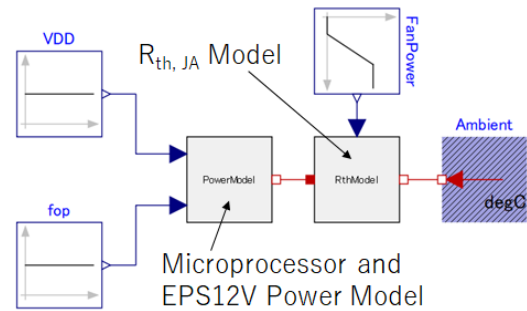


Figure 7. Modelica model connection to calculate both power and junction temperature.

Figure 8 shows junction temperature variation by fan power, changing ambient temperature. As fan power becomes higher, junction temperature becomes lower, which results in microprocessor power decrease. Figure 9 shows relationship between power consumption, junction temperature and fan power under 30 deg C ambient as an example. Not only microprocessor power but also EPS12V power decrease monotonically by fan power increase.

EPS12V power is dominant and occupies more than half of total power which PSU (Power Supply Unit) provides. To consider system-level power optimization, not only EPS12V power but also fan power should be taken into account. Thus, sum of EPS12V power and fan power (hereafter, target power) is checked as shown in Fig. 10. Fan power is relatively small, however, target power has the minimum value. Figure 11 shows derivative of target power. Target power becomes minimum when its derivative becomes zero. Optimum fan power which shows minimum target power is ~0.84 W at $T_A = 10$ deg C, ~0.93 W at $T_A = 50$ deg C, respectively. This means an optimum working point moves by ambient condition. Since application workload with usual application software varies time by time, fan needs to be controlled time by time. Optimum working point under lower workload scenario can be obtained by applying the same methodology.

6 Transient Simulation

Under steady state condition, optimum fan power is obtained easily with a few Modelica components. Instead, fan control simulation is required to obtain optimum target power under transient state condition because temperature doesn't change immediately and temperature variation is delayed by the effect of heat capacitance along heat transfer paths. Thus, heat transfer path modeling should be carefully for transient simulation and is discussed in this chapter.

Transient heat transfer path can be obtained by extending thermal resistance to RC network. There are two RC network topologies; Cauer and Foster. Cauer RC thermal network is employed in this paper (Fig. 12). To determine R_{th} and C_{th} values, measurement is conducted in the case that microprocessor starts to execute eight M172031 modules from idle state on the target computer system and fitting is executed to minimize the equation:

$$eval = \sqrt{\frac{1}{t} \int_0^t (T_{J,measured} - T_{J,estimated})^2 dt} \quad (7)$$

Here, t is the total execution time (250 sec), $T_{J,measured}$ is junction temperature obtained from measurement and $T_{J,estimated}$ is junction temperature obtained from Cauer

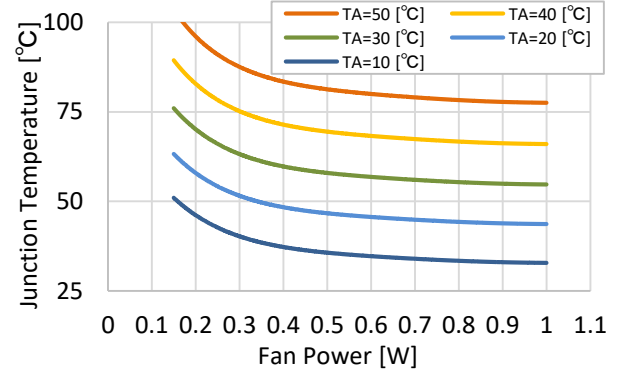


Figure 8. Relationship between microprocessor's junction temperature and fan power.

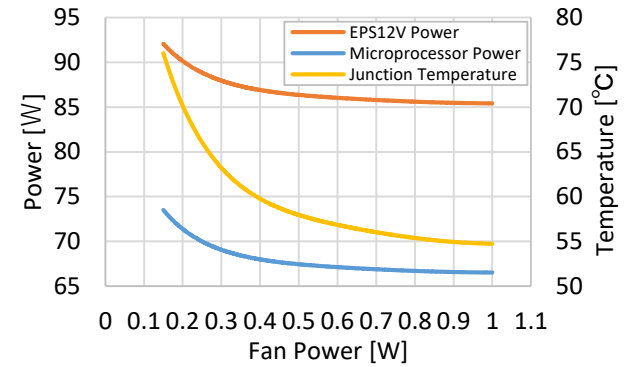


Figure 9. Relationship between microprocessor related power consumption and fan power under 30 deg C ambient.

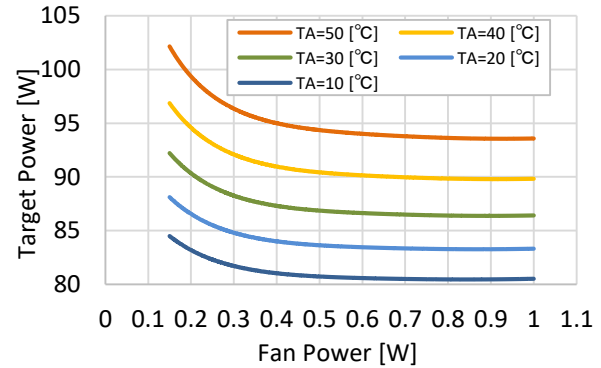


Figure 10. Relationship between sum of "EPS12V power and fan power" and fan power.

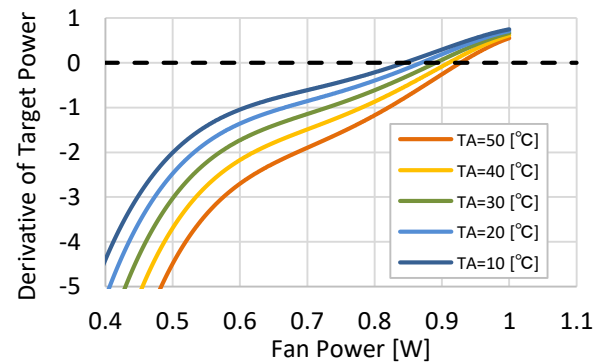


Figure 11. Derivative of sum of "EPS12V power and fan power" curve.

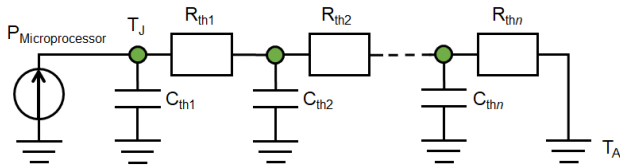


Figure 12. Cauer RC thermal network.

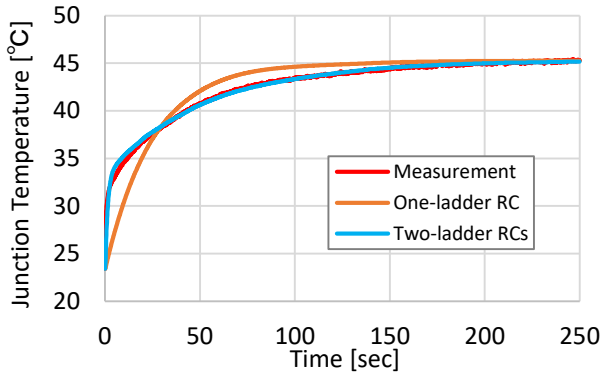


Figure 13. Transient curve of microprocessor junction temperature.

RC thermal network.

Figure 13 shows fitting results with one-ladder and two-ladder Cauer RC network utilizing OpenModelica. One-ladder RC network shows obvious difference from measurement, while two-ladder RC network fits well compared to one-ladder RC network. By adding more ladders, estimated junction temperature will fit more with measurement. Transient fan control optimization with Cauer RC network will be the future work of this research.

7 Conclusions

This paper investigates power optimization of microprocessor dedicated power rail, EPS12V, targeting a desktop computer system under a constant CPU-intensive workload condition. Microprocessor and EPS12V power models and heat transfer path model as a variable thermal resistance by fan power are created as Modelica components based on measurement data. By connecting them each other, and optimum fan control condition is explored. It is found that an optimum fan working point exists to minimize sum of EPS12V and fan power. By extending a variable thermal resistance to Cauer RC thermal network, transient heat transfer path is modeled. Transient fan control optimization with Cauer RC network will be the future work of this research.

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