

Semiconductor Package Thermal Impedance Extraction for Modelica Thermal Network Simulation Combined with VHDL-AMS model

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Abstract

Because of the emerging market demand for higher power with higher efficiency for the power semiconductor devices, thermal design of the semiconductor package and its cooling method has become one of the key elements for the power supply systems in power electric design. Thus, many thermal designers now require the junction-to-case thermal Impedance $Z_{\theta JC}$ since it is one of the most important thermal characteristics of semiconductor devices and thus, in November 2010, the more reliable and sufficiently reproducible measurement method without a case temperature measurement has been standardized by JEDEC as JESD 51-14

(<https://www.jedec.org/standards-documents/docs/jesd51-14-0>)

This paper shows the new feature in ANSYS simulation tool, ANSYS Electronics Desktop, which extracts $Z_{\theta JC}$ from JESD 51-14 compliant measurement data. The extracted $Z_{\theta JC}$, or its cumulative expression of thermal resistance $\sum_{i=1}^n(R_{thi})$ and capacitance $\sum_{i=1}^n(C_{thi})$ called “structure function”, is transformed to the Modelica thermal ladder network model. This Modelica model was simulated by ANSYS TwinBuilder, Multi-domain system simulator, and the junction temperature is reproduced by this simulation, that agreed well with the original measured temperature data. Further, $Z_{\theta JC}$ is split into two components, Junction-to-Die part(IC package DUT) and Heat-sink part(cold plate) in accordance with the guideline of Transient Dual Interface Measurement Procedure principle described in JESD 51-14. Then, $Z_{\theta JC}$ corresponding to IC package structure part is transformed to the VHDL-AMS model (as IC Package thermal compact model) while Heat-sink structure part is transformed to Modelica model(as testing fixture structure model) . Those models built by two well-known physical model description languages were connected with the acausal (i.e., conservative) condition in ANSYS TwinBuilder and the thermal response of the combined model is evaluated. The result of the simulation matches to the full Junction-to-Heat-sink Modelica thermal ladder network model, that ensures

Modelica and VHDL-AMS models can be connected in a single physical multi-domain system simulation environment in ANSYS TwinBuilder under the energy conservative principle, that might expand the potential applicability and the coverage for Modelica simulation for the broader application area.

Please send an email to eiji.nakamoto@ansys.com if there are any questions or suggestions regarding this paper.

Keywords: IC Package transient dual interface (TDI) measurement, IC Package Thermal Impedance, Structure Function, VHDL-AMS, Acausal Connection

1 Introduction

The new feature to extract structure function of semiconductor package is developed for ANSYS Electronics Desktop product in compliant with JESD 51-14. For its validation, comparison tests using sample measured data were implemented.

1.1 Extraction of Structure Function for IC Package and Validation Test

There are details described about Thermal Impedance $Z_{\theta JC}$ and the methodology of extracting IC Package structure function in JESD 51-14. In compliance with this JEDEC standard, the Visual C++ based software program for extracting structure function from the TDI measurement data (named TZextractor feature in ANSYS Electronic Desktop) was developed.

Dual interface measurement models, i.e. with / without thermal grease on the contact surface between Die-pad and Heat-sink , were evaluated. Fig.1 shows the result of the validation tests compared with the sample semiconductor package models in Software TDIM-MASTER¹, which serves as reference and example implementation of the algorithms described in JESD 51-14. The extracted structure functions by TZextractor are well matched to those of TDIM-Master (Figure. 1).

1.2 Thermal Network and State Space Models

Now, another IC model shown in Figure 2 (2SK2173 MOSFET, TOSHIBA) was evaluated for the further testing and validation. Initial input heating current

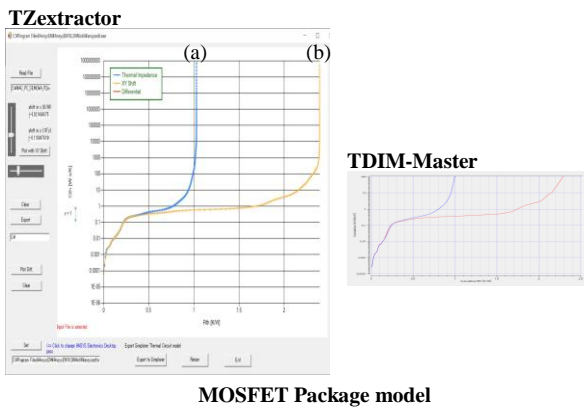
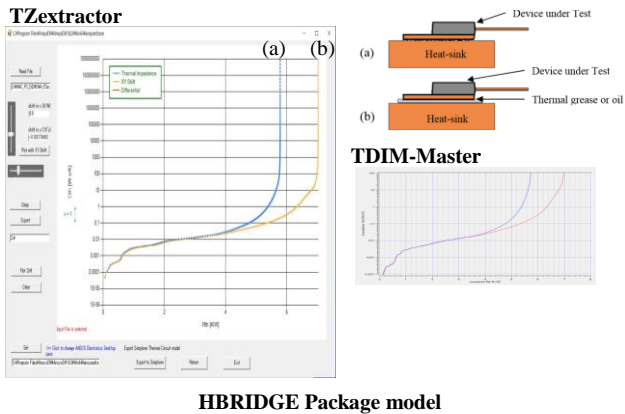


Figure 1. Structure Function by TZextractor and TDIM-Master with(b)/without(a) thermal grease for HBRIDGE and MOSFET package models



Figure 2. DUT for validation test (2SK2173 MOSFET)

and compared with the output data given by the other commercially available JESD 51-14 compliant TDI measurement system (Figure 4).

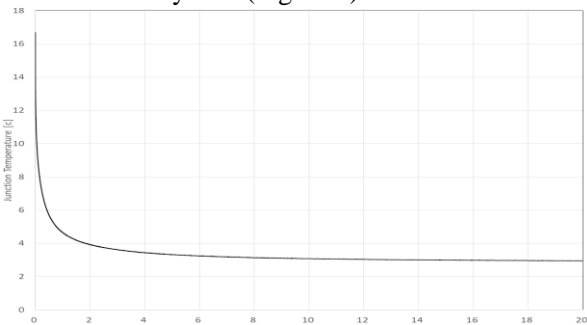


Figure 3. Junction Temperature by TDI measurement

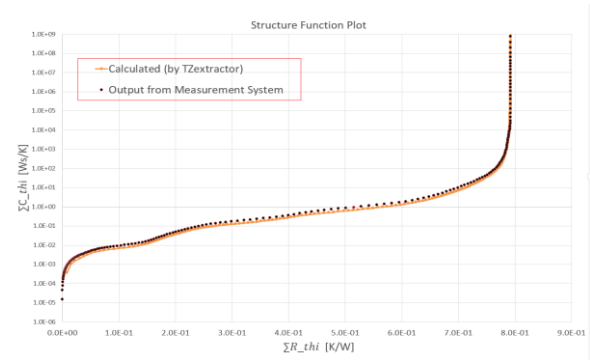


Figure 4. Structure Function of 2SK2173 MOSFET by TZextractor vs Measurement System

2. Thermal Network and State Space Models

Then, Modelica model of Cauer type thermal RC circuit network is generated from $Z_{\theta JC}$ data for 2SK2173 MOSFET model (Fig.5) in ANSYS TwinBuilder.

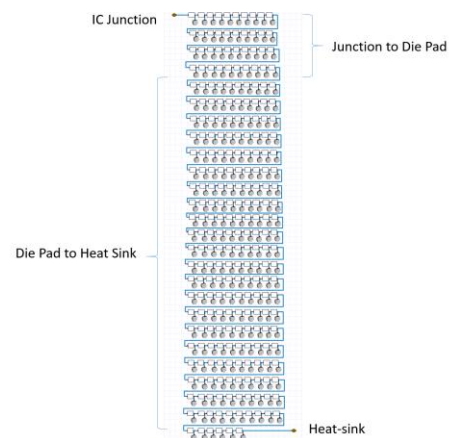


Figure 5. Thermal RC circuit network from $Z_{\theta JC}$

On the other hand, TDI measurement data of the junction temperature after power switch-off state was reversed to artificially represent the step response of the power switch-on state. Then, LTI (Linear Time Invariant) State Space mode from this step response was automatically generated as Modelica ROM (Reduced Order Model) by ANSYS TwinBuilder(Figure 6). Then, the input power of 17.14 Watt was applied for the first 100 second until the package Junction temperature reaches to the steady state temperature and then, the power was turned-off to replicate the TDI measurement condition. The junction temperature of the simulation models were monitored and compared with the TDI measurement data and the results are compared each other as shown in Figure 7.

ROM model shows good match to the measurement data after two second from switch-off while Thermal RC network model matches well from 0.5 to 1.0 second

period. However, thermal RC network models shows a slight deviation when the decreasing speed of the junction temperature becomes slowed down after one second from the switch-off until reaching to the steady state temperature. It may be because JESD 51-14 theory assumes only one directional heat flow pass between Junction and Heat-sink by thermal RC series network, that may not be good enough to represent the three dimensional thermal characteristic of the Package at the lower temperature dissipation state.

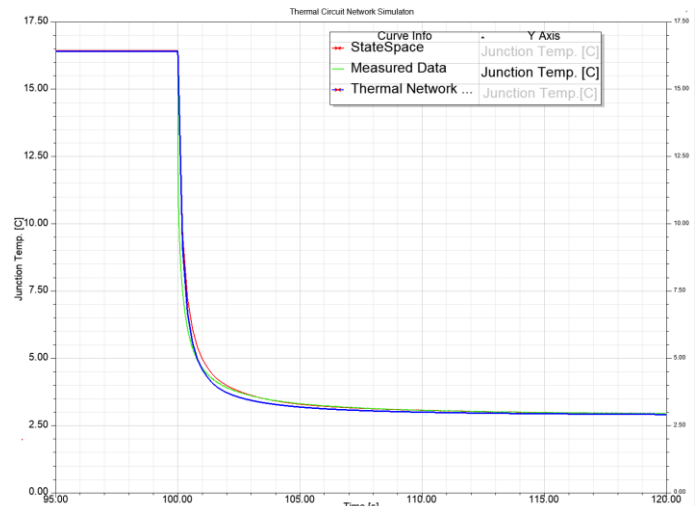
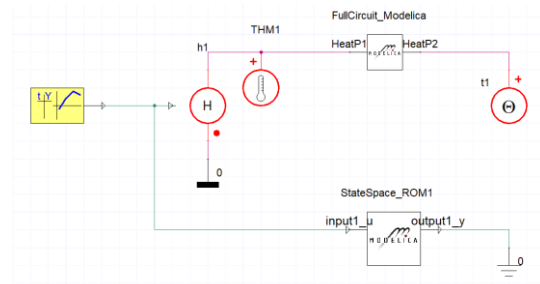


Figure 7. Junction temperature after switch-off from steady state. Simulation results of Modelica Thermal Network and State Space models compared with TDI Measurement data

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1 block StateSpace_ROM
2 "State Space ROM with Modelica format"
3 // This is the Modelica mo file for importing linear system matrices in Modelica environment
4 // Reference values are treated as extra constant inputs to the system.
5
6 Integer numofstate = 6"Number of states";
7 Integer numofinput = 1"Number of inputs";
8 Integer numofoutput = 1"Number of outputs";
9 Integer numofinput_expand = 2"Number of expanded inputs";
10
11 Real A[6, 6] = [
12   -2.2079e+003, 0.0000e+000, 0.0000e+000, 0.0000e+000, 0.0000e+000, 0.0000e+000 ;
13   0.0000e+000, -2.6134e+002, 0.0000e+000, 0.0000e+000, 0.0000e+000, 0.0000e+000 ;
14   0.0000e+000, 0.0000e+000, -2.5373e+001, 0.0000e+000, 0.0000e+000, 0.0000e+000 ;
15   0.0000e+000, 0.0000e+000, 0.0000e+000, -3.7286e+000, 0.0000e+000, 0.0000e+000 ;
16   0.0000e+000, 0.0000e+000, 0.0000e+000, 0.0000e+000, -6.4166e-001, 0.0000e+000 ;
17   0.0000e+000, 0.0000e+000, 0.0000e+000, 0.0000e+000, 0.0000e+000, -9.1913e-002
18 ];
19
20 Real B[6, 2] = [
21   1.0000e+000, 0.0000e+000 ;
22   1.0000e+000, 0.0000e+000 ;
23   1.0000e+000, 0.0000e+000 ;
24   1.0000e+000, 0.0000e+000 ;
25   1.0000e+000, 0.0000e+000 ;
26   1.0000e+000, 0.0000e+000
27 ];
28
29 Real C[1, 6] = [
30   2.1551e+002, 2.9687e+001, 4.0653e+000, 9.7089e-001, 8.2108e-002, 2.9955e-003
31 ];
32
33 Real D[1, 2] = [
34   0.0000e+000, 1.0000e+000
35 ];
36
37 Real x0[6] = fill(0, 6) "Initial conditions";
38
39 Real x[6] "State Vector";
40 Real u[2] "Expanded input Vector";
41 Real y[1] "Output Vector";
42
43 parameter Real u_ref1 = 0.0000e+000;
44
45 Modelica.Blocks.Interfaces.RealInput Input1_u;
46 Modelica.Blocks.Interfaces.RealOutput Output1_y;
47
48 initial equation
49   x = x0"Specify initial conditions";
50
51 equation
52   u[1] = Input1_u;
53   u[2] = u_ref1;
54   Output1_y = y[1];
55
56 der(x) = A * x + B * u;
57 y = C * x + D * u;
58
59 end StateSpace_ROM;

```

Figure 6. Modelica State Space Thermal model for 2SK2173 MOSFET

3 Modelica with other modeling language models

VHDL-AMS is the international standard description language registered by IEEE and ICE, that has a long history since its origin in '70 and is one of the well-known modeling languages used in semiconductor, electrical and electronics design arena. There are many open or IP protected models and libraries. Because almost all the machines, hardware products and systems are now electrically controlled by the controller (ECU, PLC) with the electrical drive trains (actuators, motors) by using power electric technology, so it shall be beneficial if Modelica simulation could be connected or has an interface to other modeling language models such as VHDL-AMS.

3.1 Modelica model combined with VHDL-AMS

To connect those two different models, an interface port that enables Modelica acausal pins interpreted to VHDL-AMS conservative pins are available in ANSYS TwinBuilder. Figure 8 is the result of the simple test for mechanical mass/spring/damping component models with different Modelica-to-VHDL-AMS combinations. As result shows, the response of mass displacement are all the same for three different model connections which ensure the validity of the interface port.

3.2 Validation check with IC package model

According to JEDEC 51-14, $Z_{\theta JC}$ can be split into two components, IC package part and Heat-sink part by TDI Measurement Procedure principle. As for the validation, test model of 2SK2173 MOSFET is evaluated. In this model, the first thirty series RC thermal network shall corresponds to IC package and the latter part of the network shall be Heat-sink according to the two different measurements (i.e. with and without thermal grease on DUT Die-pad). Then, IC package

part is made by VHDL-AMS model while Heat-sink part is made by Modelica model in ANSYS TwinBuilder. Those two different models are connected via interface ports and simulated. The simulation of combined thermal network models shows identical result to the full Modelica network model (Figure 9).

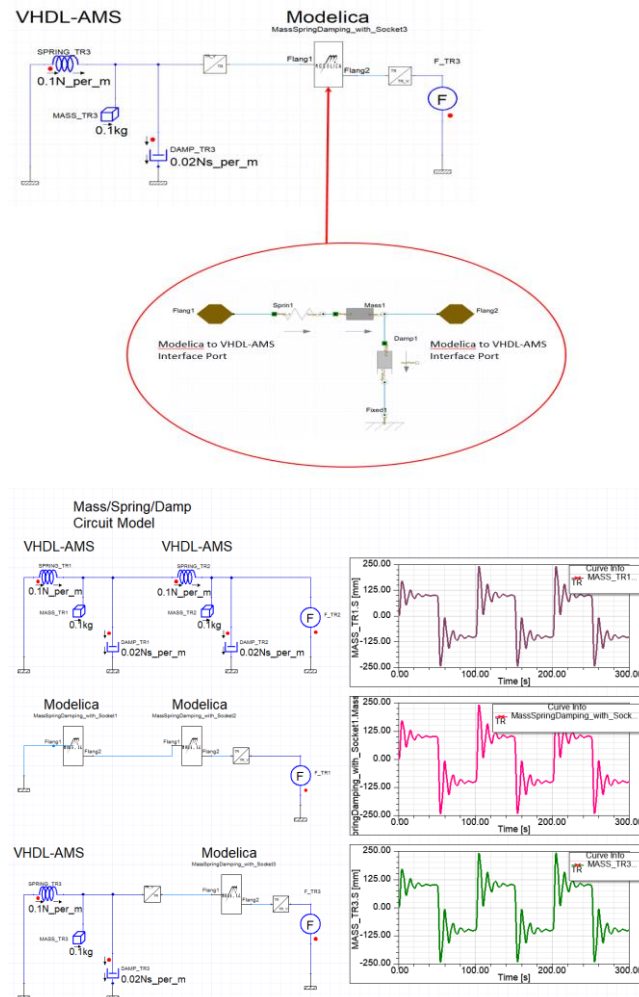


Figure 8. Mechanical mass/spring/damping component models with different combinations by Modelica-to-VHDL-AMS interface port

4 Summary

The new feature to extract Structure Function of semiconductor package was developed which is available for ANSYS Electronics Desktop product. This feature was validated by the measurement data in compliant with JESD 51-14 standard of JEDEC. Extracted result was transferred to Modelica thermal network and State Space models and the result of the thermal circuit simulations were compared with the original temperature measurement data with reasonable

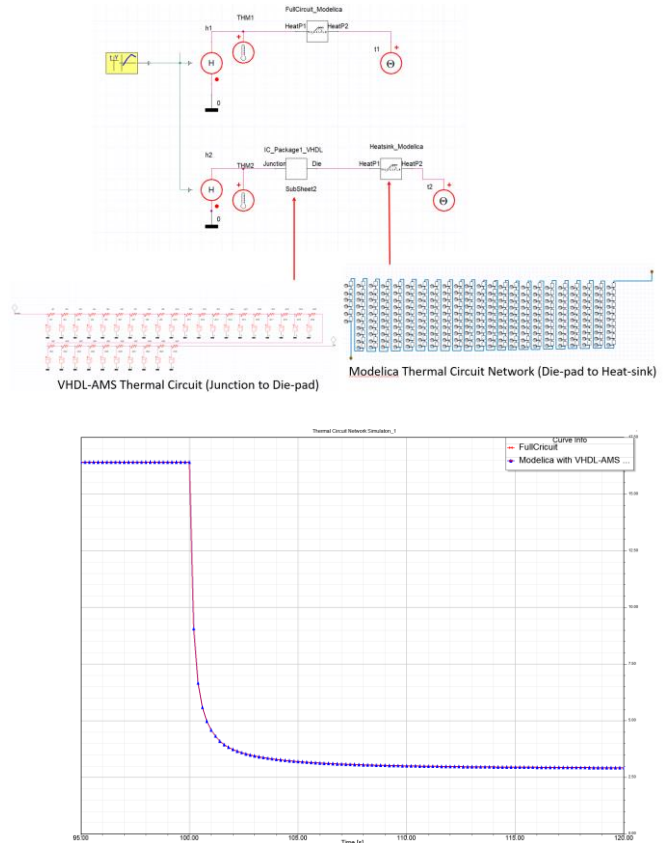


Figure 9. Combination of Modelica and VHDL-AMS thermal network components compared with full Modelica network model

correlation. Then, the extracted thermal network data was split into two thermal structure models by different modeling language, Modelica and VHDL-AMS. Those are connected via Modelica acausal to VHDL-AMS conservative interface port in ANSYS TwinBuilder. Result of the combined model simulation identically matched to the full Modelica thermal network model.

Acknowledgements

Modelica thermal network model for semiconductor package can be created from JEDEC JESD 51-14 standard measurement, that is useful to evaluate its thermal characteristics by thermal network circuit simulation. The network model can also be created for other modeling language such as VHDL-AMS.

Combination of VHDL-AMS models with Modelica may be useful to expand its applicability and coverage for broader application area.

References

1. D. Schweitzer, Software TDIM-MASTER: Program for the evaluation of transient dual interface measurements of Rth-

JC. This software serves as reference and example implementation of the algorithms described in this standard and can be downloaded from the JEDEC homepage: <http://www.jedec.org>.

2. JEDEC JESD51-14, “Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction-to-Case of Semiconductor Devices with Heat Flow Through a Single Path”, 2010