From Low-Cost High-Speed Channel Design, Simulation, to Rapid Time-to-Market

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Abstract

Leadframe packages are always adopted as the low-end devices. When the low-cost channel including the leadframe package and the two-layer PCB is required for high-speed digital signaling over 1 Gb/s, the iteration of full channel simulation and analysis with reliable EDA tools should be taken before the device is rolled out. Different channel designs were characterized in the frequency domain using the 3-D full-wave electromagnetic field solver to analyze the bottleneck of channel performance. Comparison of the full channel S-parameters, the channel with the proposed DDR3 memory controller package suffers less insertion loss. The chip-package-board co-simulations in the time-domain using the chip HSPICE netlists and full channel S-parameters for the DDR3 data accessing at 1.2, 1.4, and 1.6 Gb/s were taken and demonstrated that the channel including the proposed package design had larger timing and voltage margins, and less jitter, overshoot and undershoot, which all conform to JEDEC Standard. The waveform measurement also verified the same prediction that the DDR3 memory controller encapsulated in the modified E-pad LQFP package achieved no cost impact and enough timing margin up to 1458 Mb/s. The performance of mature leadframe packages can be promoted if the careful package designs are taken.

Keywords: DDR3, E-pad, LQFP, return path, S-parameters, jitter, eye diagram, JEDEC

1 Introduction

Before 2009, the year of DRAM transition from DDR2 to DDR3, several famous fabless semiconductor companies predicted that the DDR3 memory controller should be designed and encapsulated with the flip-chip ball grid array (BGA) package because the wire-bonding packages induce large inductance or impedance that is harmful to the single-ended DDR3 signals accessing over 1 Gb/s. The low price is always the king for the consumer electronics market, such as LCD TVs, BD players and broadband Wi-Fi routers, even though the low-cost 2-layer PCB would be implemented. In the following years, many design guides and studies have been proposed to recommend wire-bonding or flip-chip BGA packages for the DDR3 memory controller (Micron Tech., 2009; Texas Inst., 2014; Shah, 2012; Synopsys Inc., 2009). However, few papers presented the investigation of DDR3 memory controller encapsulated with the wire-bonding leadframe packages. In this paper, several passive channels were designed and studied whether the memory controller with the exposed die-pad (E-pad) low-profile quad flat package (LQFP) was acceptable to access data rate up to 1.6 Gb/s using the chip-package-board co-simulation in frequency and time domains. The effects of different return paths in the memory controller package were characterized with the 3-D full-wave electromagnetic field solver to demonstrate the bottleneck of channel performance. Finally, the DDR3 waveform measurement in the practical platform was taken matching the previous co-simulation prediction of signal integrity. The reliable simulation tools are very important to analyze the channel performance for different designs that can predict the effects of nonideal return paths correctly and is helpful to finalize the channel design and expedite time-to-market.

2 Package Structures

Leadframe packages are made of the single-layer copper-based alloys. Thus, they are cheaper but suffer worse electrical performance, including larger cross-talk and energy loss due to longer parallel leads and bondwires, compared to the ball grid array (BGA) packages with at least two-layer substrate. Figure 1 shows the structure of exposed die-pad (E-pad) low-profile quad flat package (LQFP) with 256 pins. In order to increase the signal inputs/outputs interconnected between the chip and external devices on the PCB, all ground wires are bonded onto the ground bar, which connects with the E-pad through the bridges or the connecting bars. Then the E-pad soldered with the ground pad of PCB connects to the global ground. Another benefit for the E-pad is to promote the heat dissipation. If the ground wires are bonded onto the E-pad top surface, moisture may easily penetrate into the package through the interface between the molding compound and the E-pad. In addition, there is a reduction in the coupling strength of the E-pad to the

molding compound. As a result, an interface peel-off phenomenon caused by thermal stress may occur (Choi, 2002). Accordingly, the ground wires are disconnected from the E-pad. That is why all the ground wires from the chip shall be bonded onto the ground bar, which is elevated from the package bottom surface.

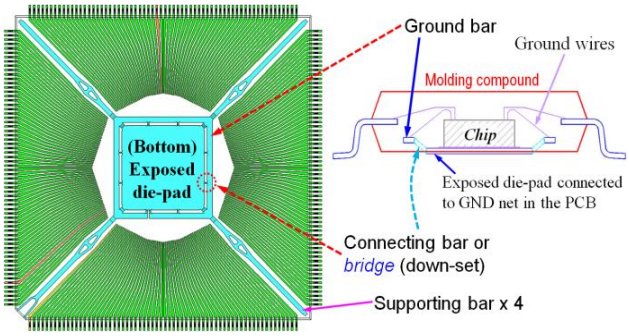


Figure 1. Top and side views of 256-pin E-pad LQFP package.

3 Co-Simulation Methodology

The passive channel design is critical to maintain the signal and power integrity of high-speed digital signals, especially for the package design. In order to ensure the acceptable channel performance, the iterative co-simulation using the reliable EDA tools were taken. Both the chip netlists of DDR3 memory controller and DRAM cascaded with the wideband channel S-parameters including the power and signal nets are modeled for the transient analysis, as shown in Figure 2. The chip input/output buffer information specification (IBIS) models are not recommended because those behavior models are less accurate for the signal speed over 1 Gb/s.

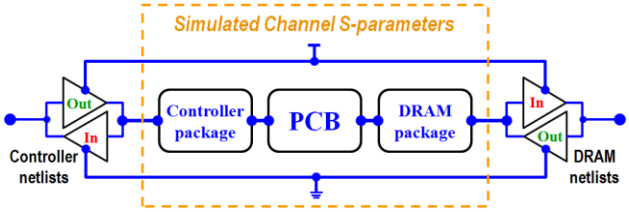


Figure 2. Channel models of DDR3 interface co-simulation.

4 Channel Analysis

The low-cost DDR3 channel configuration includes the memory controller package, the PCB and the DRAM package, as shown in Figure 3. Two facts the fabless chip companies are unable to change. The first fact is that the DRAM package type and ball pins are defined by JEDEC Standard (JEDEC Std., 2012). The second fact is that many original equipment manufacturers (OEM) always choose the 2-layer PCB rather than the 4-layer PCB due to 40% cost reduction, as listed in Table 1 (Chen, 2009). Finally, the fabless chip companies only can determine the memory controller package type. According to the package cost comparison listed in Table 2 (Chen, 2009), the adoption of leadframe packages can save up to 92−208% in package cost. The challenge is whether the full channel performance is acceptable for the data access over 1 Gb/s. In order to realize the performance difference of the memory controller encapsulated in the leadframe and the BGA packages, both full channel S-parameters including the DDR3 signal and the I/O power net (1.5 V) were extracted using ANSYS HFSS, a 3-D full-wave electromagnetic field solver, and then cascaded with the chip netlists for the transient analysis in Synopsys HSPICE. As demonstrated in Figure 4 obviously, the channel with the conventional E-pad LQFP has larger skew and insufficient timing margin compared to that with the BGA package. How to improve the E-pad LQFP performance became a must.

Table 1. Examples of PCB cost ratios in digital TV mother boards.

Type / Item	Model-X TV		Model-Y TV	
	2-layer PCB	**4-layer PCB**	**2-layer PCB**	**4-layer PCB**
	Cost Ratio	Cost Ratio	Cost Ratio	Cost Ratio
Controller chip	37.2%	34.7%	26.7%	24.9%
PCB	**9.3%**	**15.4%**	**9.1%**	**15.1%**
Other components	53.5%	49.9%	64.3%	60.0%

Table 2. Cost ratio comparison among different package types.

Package Type	Size (mm)	Cost Ratio	Remarks
E-pad LQFP216	26 x 26	**0.77**	216 pins.
E-pad LQFP256	30 x 30	**1.00**	Comparison baseline.
PBGA (2-layer)	27 x 27	**1.92**	With plating lines.
PBGA (2-layer)		**2.12**	Without plating lines.
PBGA (4-layer)		**2.12**	With plating lines.
PBGA (4-layer)		**2.31**	Without plating lines.
FC-BGA (4-layer)		**3.08**	Exclusive of bumping cost.

5 Improved Leadframe Package

Several simulations of full channel S-parameters were taken including the E-pad LQFP package with different ground bar widths, bridge widths and numbers. Figure 5 shows the partial pictures of E-pad leadframe packages with different bridge numbers. Finally, the bridge number is the key factor to improve the channel performance. As package modeled with different numbers of bridge shown in Figure 6, the simulation results indicated in Figure 7 that the package with more bridges suffers less insertion loss than that with fewer bridges. The improved amplitude is 3 dB at 1.3 GHz. The bridges connected between the ground bar bonded with the ground wires from the chip and the exposed pad (E-pad). The more the bridges, the smaller return loop

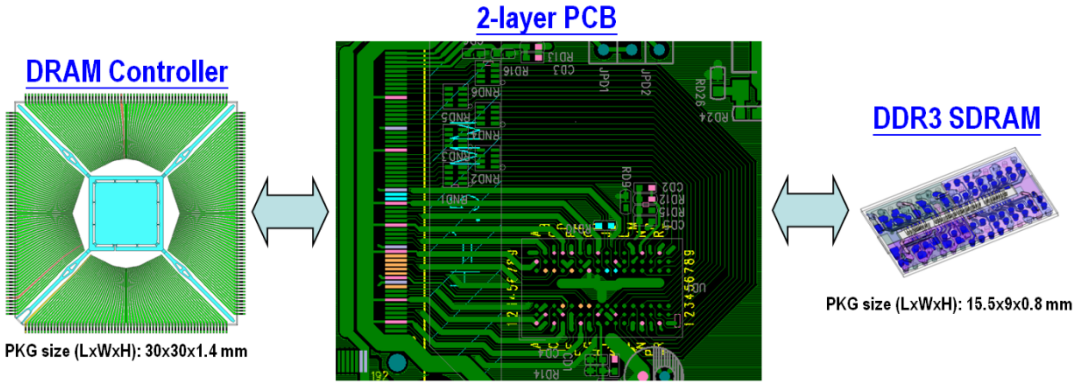
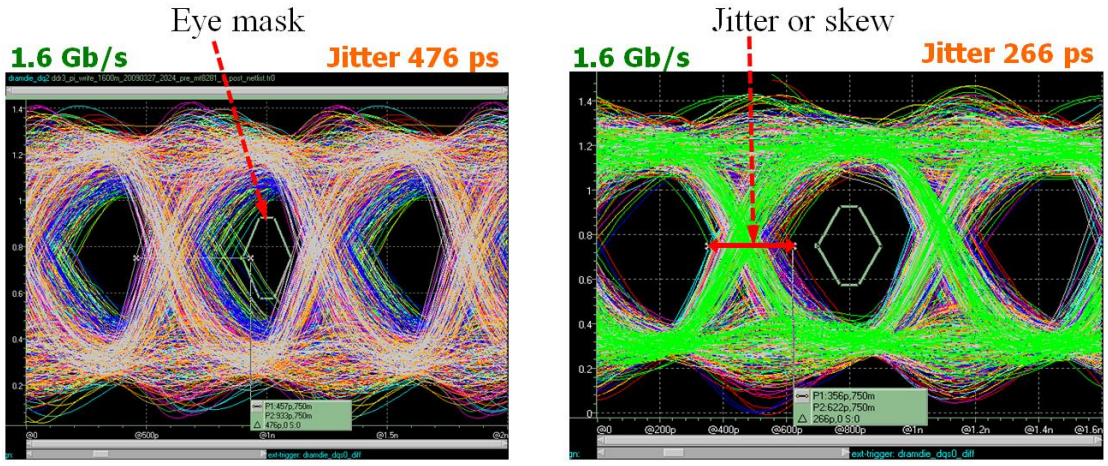


Figure 3. Low-cost DDR3 channel configuration.



(a) (b)

Figure 4. Simulated DDR3 eye-diagrams of overlapping 1-byte signals on DRAM chip side for writing data at 1.6 Gb/s. (a) Memory controller in conventional E-pad LQFP. (b) Memory controller in BGA package.

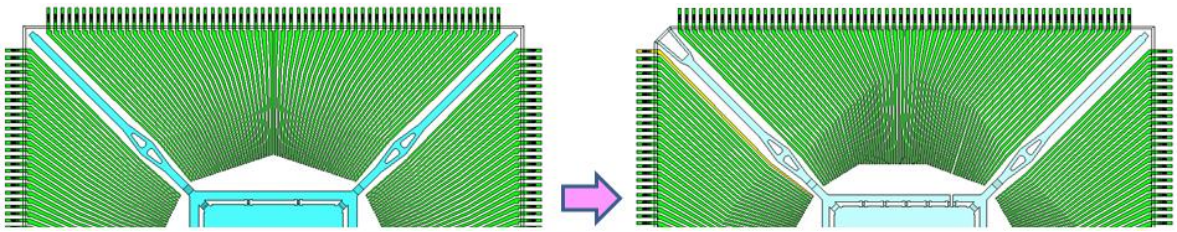
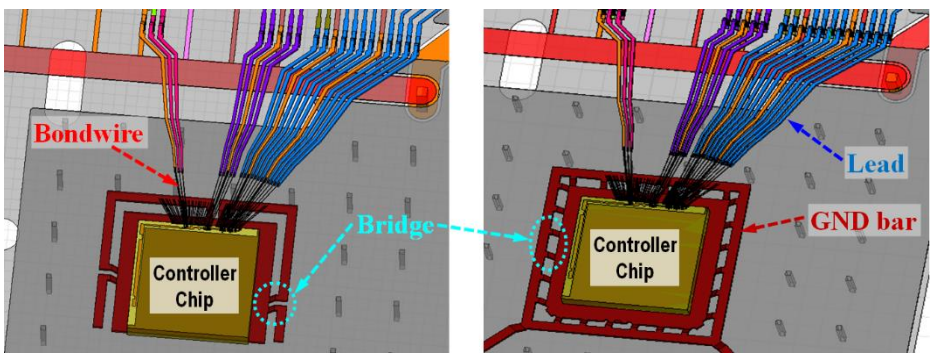


Figure 5. Modification of E-pad leadframe packages with different bridge numbers.



(a) (b)

Figure 6. Simulation models of memory controller packages. (a) E-pad LQFP with few bridges. (b) E-pad LQFP with many bridges.

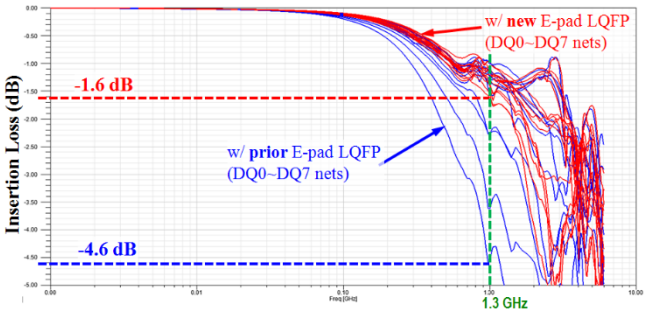


Figure 7. Insertion loss comparison of simulated channel S-parameters for DDR3 DO0-7 nets. Red curves are for the package with more bridges and blue curves are for the package with fewer bridges.

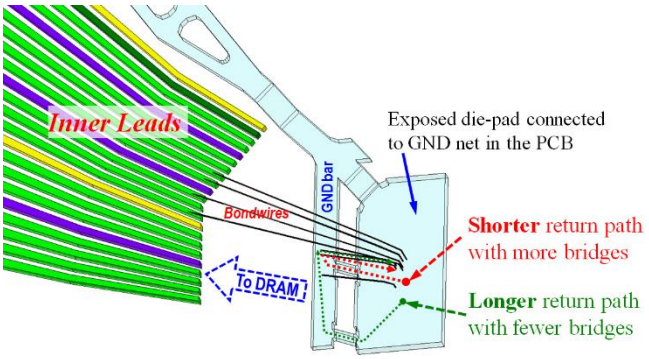


Figure 8. Return paths of high-speed signals in E-pad LQFP package.

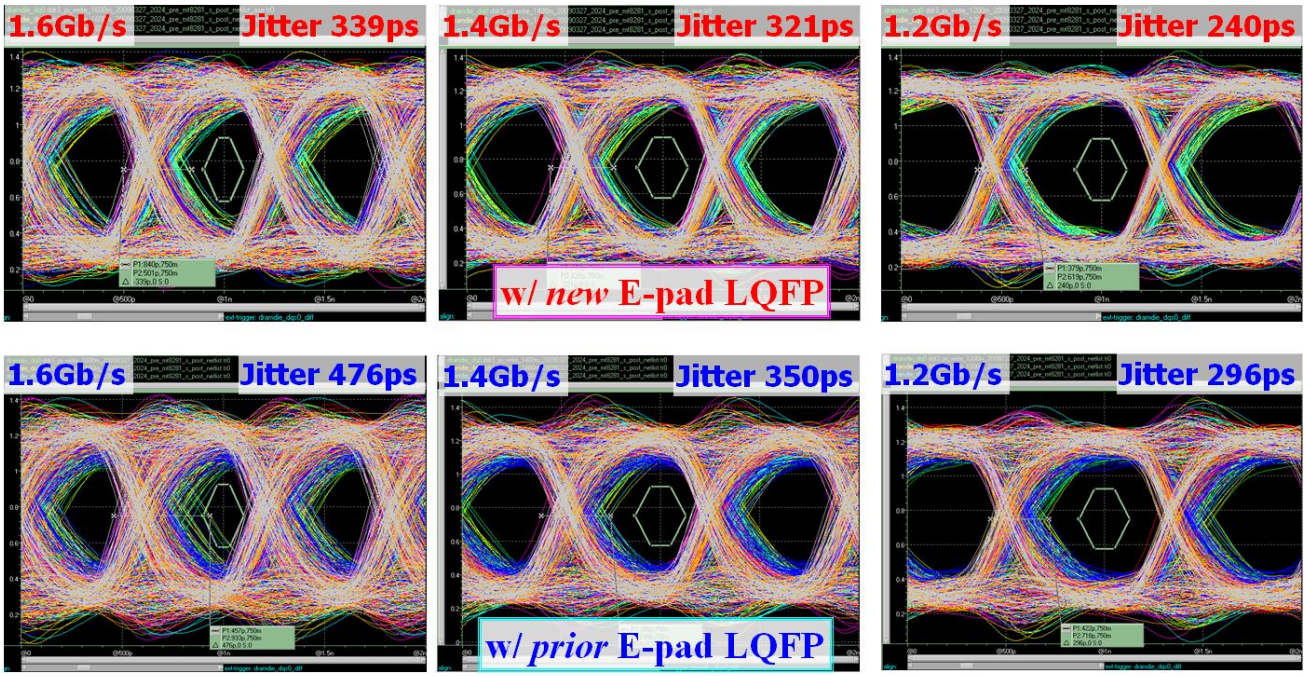


Figure 9. Simulated DDR3 eye-diagrams of overlapping 1-byte signals on DRAM chip side for writing data at 1.2, 1.4, and 1.6 Gb/s respectively. The E-pad LQFP with many bridges is in the upper charts and with few bridges is in the lower charts.

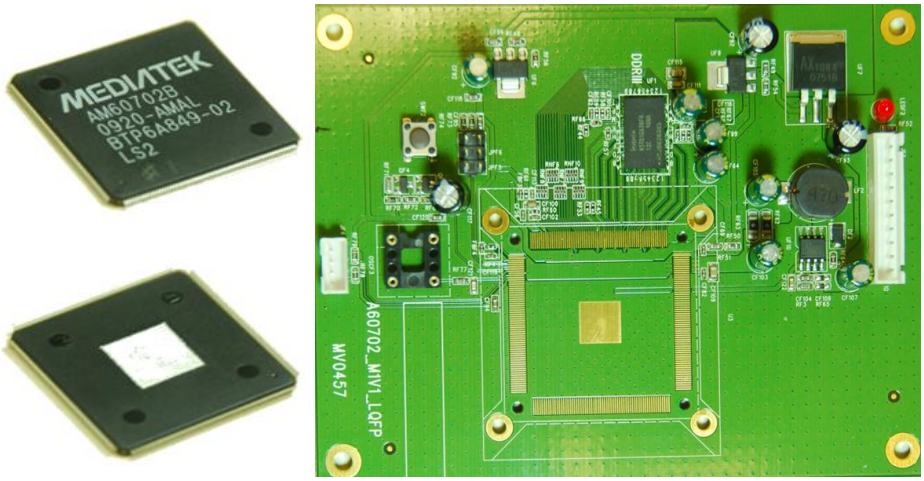


Figure 10. The practical E-pad LQFP package and 2-layer test board for DDR3 waveform verification.

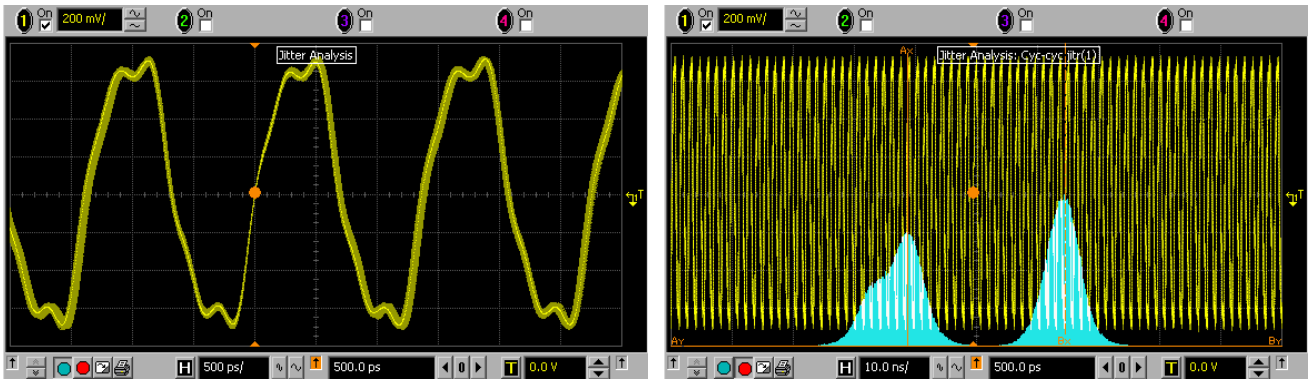


Figure 11. Measured DDR3 differential clock waveform at 729 MHz without data access (idle state) for 50.5% pulse width and tJIT (cc) for -59.4 to 56.9 ps.

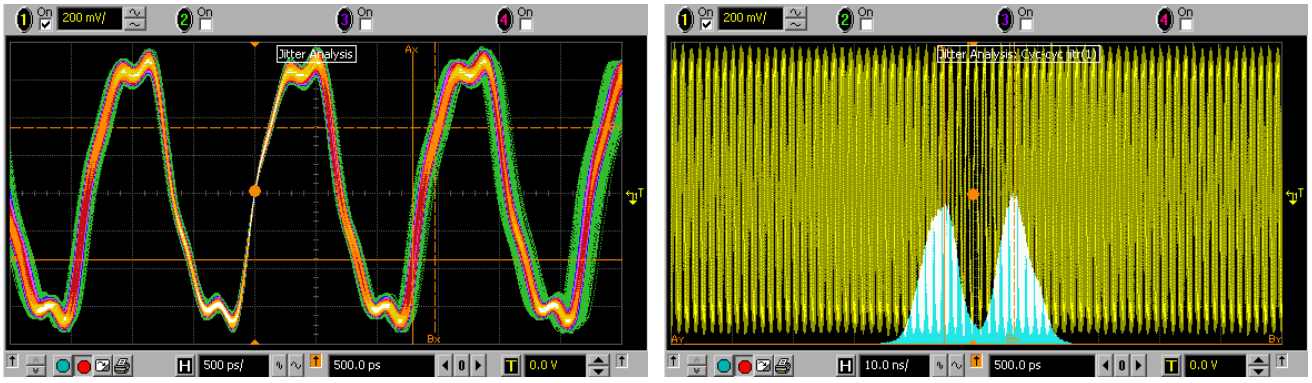
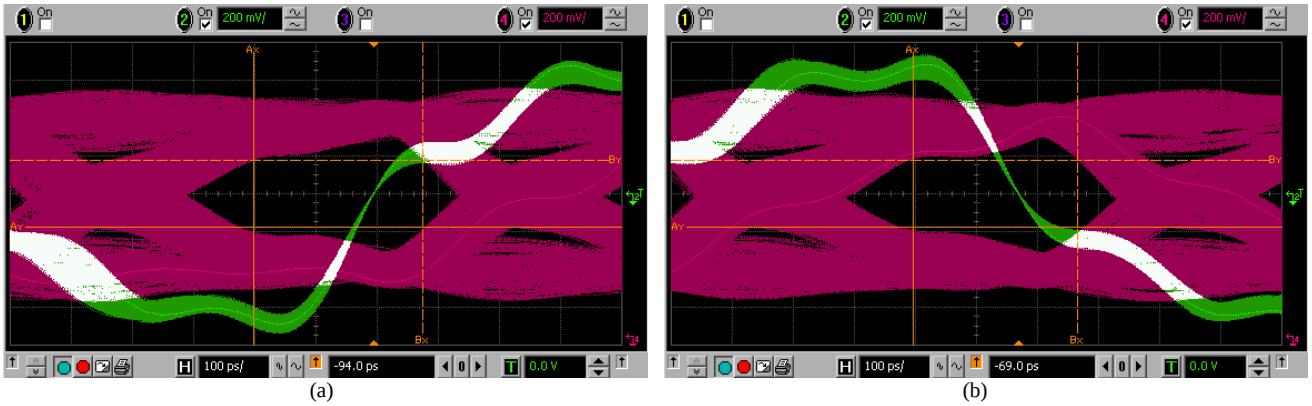


Figure 12. Measured DDR3 differential clock waveform at 729 MHz with specified data access (special test patterns) for 50.5% pulse width and tJIT (cc) for -93.0 to 90.1 ps.



(a) (b)

Figure 13. Measured DDR3 DQ14 writing waveform at 1458 Mb/s with 65 Ω drive strength for timing window. (a) 276 ps triggered by rising DQS. (b) 270 ps triggered by falling DQS.

or path is, as illustrated in Figure 8. Accordingly, the smaller the wire loop or area, the smaller the wire inductance or impedance is. That is due to high-speed or high frequency return currents follow the path of least inductance. The longer the return path, the more high-frequency components filtered out it will slow the edge rate (Johnson, Graham, 1993; Hall *et al*, 2000; Young, 2001).

Less insertion loss of full DDR3 channel in the frequency domain would expect larger eye-open in the time domain. Figure 9 demonstrates the compared DDR3 eye-diagrams between before and after package modification. Improved timing window is obviously for the new E-pad LQFP, especially for the data rate at 1.6 Gb/s. Reduced data jitter or skew achieves the larger timing margin due to less insertion loss causing less edge rate degradation. Based on the acceptable co-simulation results, there was more confident to assemble the real chip for the following verification. Leadframe packages can be manufactured using the stamping or etching process. Therefore, increase of bridge number in the package is without any cost impact.

6 DDR3 Waveform Verification

The memory controller chip was made using tsmc 40-nm process node, assembled with the modified E-pad LQFP256 package and mounted on the 2-layer test board, as shown in Figure 10. The test conditions are as follows:

1) PCB: 2 layers, 1.6 mm thickness; signal trace width/space = 5/20 mils.
2) Power supplies: 1.05 V for the core power (V_{CCK}) and 1.5 V for the I/O power (V_{CCIO}).
3) DRAM: Hynix DDR3-1600 1Gb (x16, H5TQ1G63BFR), FBGA96 package.
4) Access rates: Clock/DQS at 729 MHz and DQ/DM at 1458 Mb/s.
5) Clock (parallel) termination: 100 Ω near the DRAM.
6) Interface settings: 60 Ω ODT and 40 Ω drive strength for DRAM; 120 Ω ODT and 65 Ω drive strength for memory controller.

Figure 11 shows the differential clock waveform measured on the parallel termination (100 Ω) when there is no data access (idle state). The measured pulse width (tCH) and cycle to cycle period jitter (tJIT, cc) are 50.5% and -59.4 to 56.9 ps, respectively. When the data access with the special test patterns, the measured tJIT becomes worse, as shown in Figure 12, when all high-speed data nets start to switch resulting in larger voltage droop on the I/O power due to simultaneous switching noise (SSN). Although adding more board capacitors would stabilize the I/O power, the result was insignificant due to the high power impedance with limited power leads assigned in the E-pad LQFP256 package. The writing data (DQ14) waveform was measured near the DRAM on PCB without significant overshoot and undershoot as shown in Figure 13. This phenomenon is same with the co-simulation predicted in Figure 9. The measured timing window (setup + hold time) is around 270 ps. Eventually, All the measurement data conform to JEDEC Standard (JEDEC Std., 2012).

7 Conclusions

The co-simulation flow using the reliable simulation tools to predict the high-speed channel performance fast is presented. The modified E-pad LQFP256 package with more bridges was proposed resulting in shorter return path and achieved better timing window in the low-cost high-speed channel. All the measured waveforms meet JEDEC specification. In 2010, we rolled out the first digital TV SoC encapsulated in the E-pad LQFP256 package accessing DDR3 data rate over 1.3 Gb/s on the 2-layer PCB in the world. The next challenge is to study if the DDR4 channel could be implemented with the leadframe package.

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