RESEARCH AND DEVELOPMENT OF A SIC STATIC INDUCTION TRANSISTOR

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ABSTRACT

A fabrication process for SiC Static Induction Transistors (SITs) is developed and tested. Simulated and measured results of the device are presented. The complete fabrication process involves only 5 lithography steps, due to the self-aligned process used for mesa, ohmic contacts and gates. This makes the process fast and minimize the risk of process errors. Only optical lithography is used in the process, why dimensions are not optimised. Mesa widths of 2, 3, 4 and 5 µm are processed. Since the process is scalable, better performance can be expected with smaller widths achieved by the use electron beam lithography. Preliminary results indicate FET operation with a maximum current density of 110 mA/mm.

INTRODUCTION

A SIT is a vertical short-channel MESFET, where both the gate and drain voltage control the current. Its major advantages are its high power density, approaching 300 kW/cm^2 [1], and its high frequency performance with a cut-off frequency (f_T) of 7 GHz [2].
Under pulsed power test conditions it has delivered a maximum output power of 900 W at 425 MHz with a drain efficiency of 78% and 14 dB associated gain. 900 W output power are also reached at 1.3 GHz, the efficiency and associated gain are then 65 % and 11 dB, respectively [3].
SiC is very well suited for this high-power, high frequency device. Its high critical electric field, high-saturated electron drift velocity and high thermal conductivity are very useful for the SITs properties and make an excellent match.

DEVICE STRUCTURE

The schematic structure of the manufactured and simulated SIT is shown in Fig. 1. The manufactured devices are on 4H-SiC conducting substrate from Cree Research (n-doping 3.5 x 10^{17} cm^{-3}, thickness 385 µm). On top of the substrate are a highly doped buffer layer (n = 1 x 10^{19} cm^{-3}, 0.3 µm), a moderately doped drift layer (n = 7 x 10^{15} cm^{-3}, 4 µm) and a highly doped contact layer (n = 1 x 10^{19} cm^{-3}, 0.3 µm). The current flows vertically between source and drain through the drift region when a drain voltage is applied.

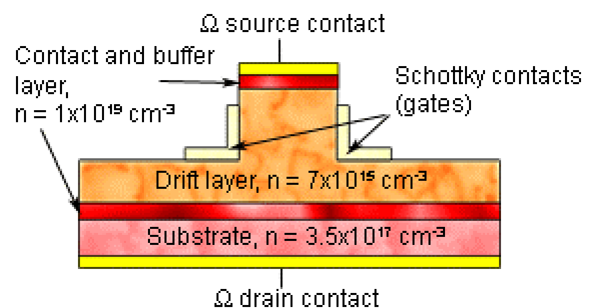

Figure 1. Schematic structure of a SIT

DEVICE FABRICATION

The backside drain contact is formed first by evaporation and annealing of 1500 Å Ni. The mesa step begins with an evaporated Ni/Ti/Ni layer, formed with photolithography and a lift-off process. The fingers are formed with Inductively Coupled Plasma (ICP) etching with NF_3 and O_2 (Fig. 2a). The etch rate is 0.5 µm/min, the walls are vertical and the surface is not visually damaged [4]. The mesa height after etching is 2 µm.
The etch mask is then used as a self-aligned source metalization, which is then annealed to form the ohmic contacts. To form the gates, a Ti/Au layer is sputtered over the whole surface. The sample is then etched with Ar ion beam in an angle, by using the mesa fingers as a shadow mask, protecting the trenches and walls (Fig. 2b), forming the gate structures. This has to be done from both sides (Fig. 2c), with Reactive Ion Beam Etch (RIBE).

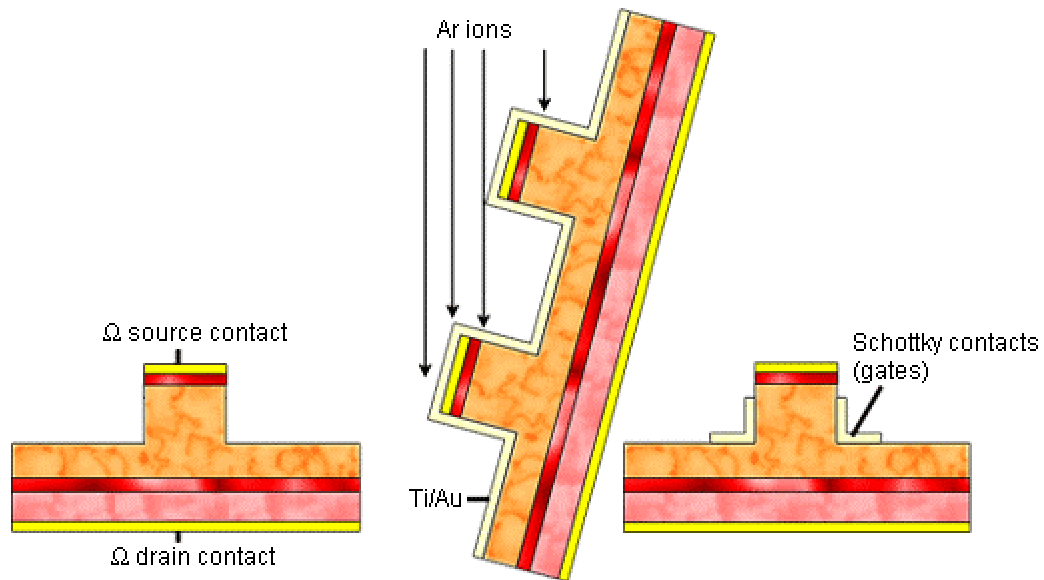

Figure 2a-c. Schematic illustration of the basic fabrication steps.

SiO_2 is then sputtered on the surface to isolate the pads from the conducting substrate (Fig. 3a). A resist mask is used to wet etch the active areas of the device. The source and gate pads are defined with a lift-off process with evaporated Ti/Au (Fig. 3b).
Airbridges are fabricated with two lithography steps; the first one to align the mesa tops and sputter a thin Au layer. The second lithography followed by Au plating forms the actual bridges (Fig. 3c).

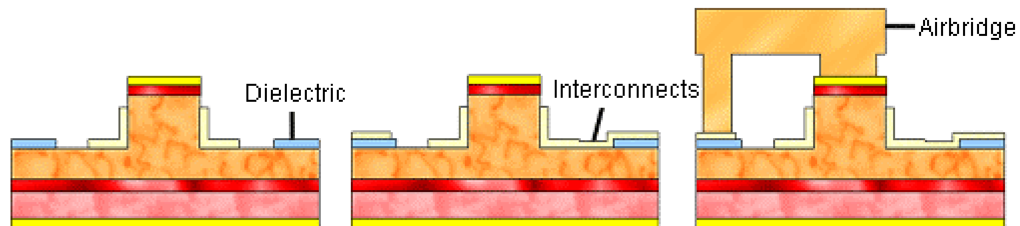

Figure 3a-c. Schematic illustration of the basic fabrication steps.

The fabricated transistors have 1, 2, 4 and 8 fingers, and the mesa and trench widths are varied.

SIMULATIONS

All simulations are performed with ISE TACD, a very good tool for testing and realising the possibilities and problems with certain structures. ISE TCAD is used to optimise device parameters such as doping, distances and layer thicknesses [5]. Results from simulations show that current

densities of above 90 mA/mm can be expected with a source width of 2 µm. I_d versus V_d is shown for this case in figures 6. The potential in the component and the electron density are also shown (Fig. 4 and 5).
The parameter values for the simulated structure are shown in Table 1.

Source width:	4 µm
Trench width:	5 µm
$N_{D,epi}$:	$7x10^{15}$ cm^3
$N_{D,sourcre\ \&\ drain}$:	$1x10^{19}$ cm^3
Mesa height:	2 µm

Table 1. Parameters used in simulations.

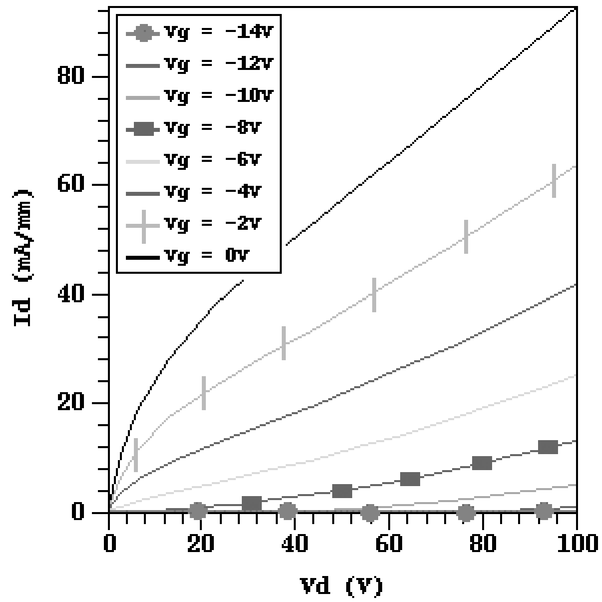

Figure 4. IV plots for SIT with mesa width 4 µm.

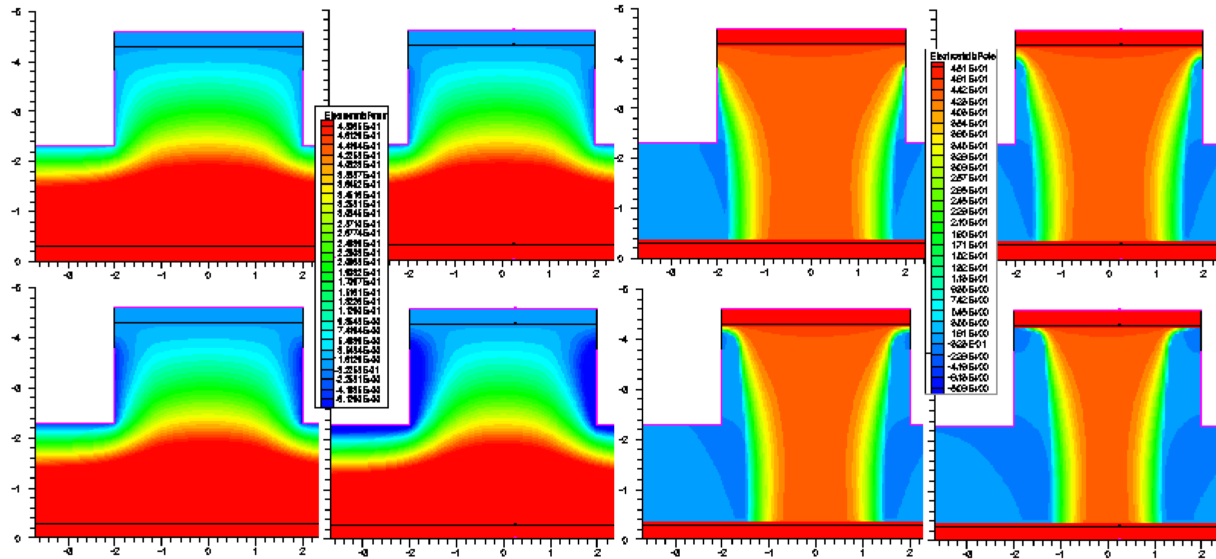

Figure 5a-b. Potential (a) and e^--density (b) for SIT with mesa width 4 µm. Vg is 0, -4, -8 and –12V

RESULTS

So far, the process is proven functional and gate control, FET operation and a maximum current density of 110 mA/mm are achieved (Fig. 5).
The gate Schottky contacts show diode characteristics, but with rather high turn-on voltage and rather low reverse breakdown voltage.

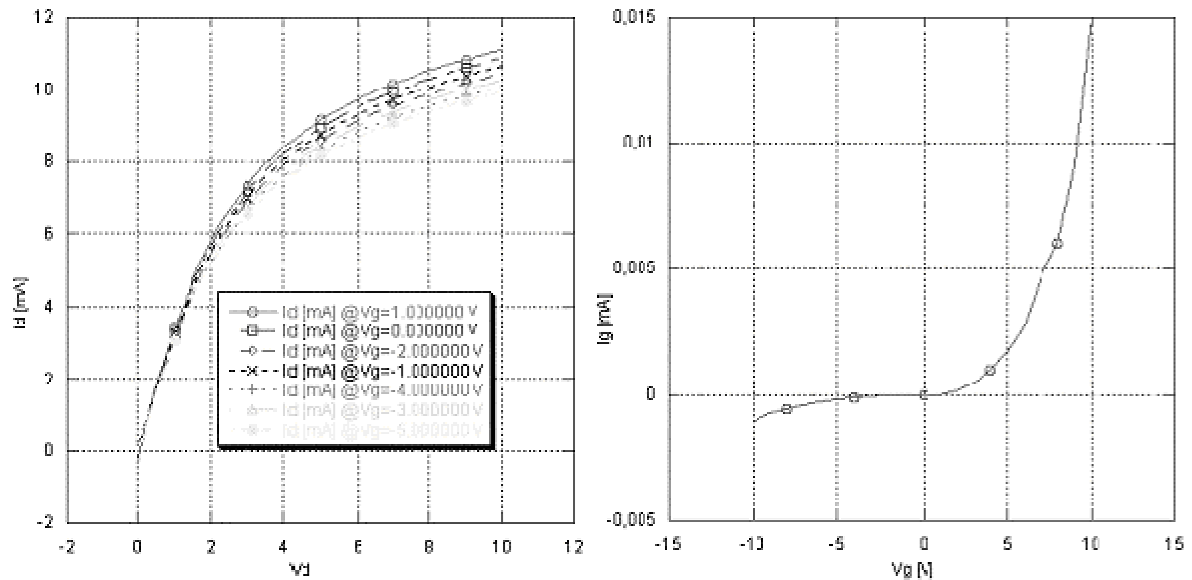

Figure 5. Results with 2 finger device, mesa width 4 µm.

SUMMARY

This fabrication process is not optimised concerning device dimensions, and only optical lithography is used. By the use of e-beam lithography, primarily for the pad-gate connection and the first airbridge step, the dimensions could shrink and the performance increase. So far, the process is functional, but improvements should be expected. The major advantages with the process are the low number of lithography steps required. This makes the process fast and minimize the risk of processing errors.

REFERENCES

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