

An Active Recursive RF Filter in 0.35 μm BiCMOS

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ABSTRACT

An active recursive filter approach is proposed for the implementation of an inductorless, tuneable RF filter in BiCMOS. A test circuit was designed and manufactured in a 0.35 μm SiGe BiCMOS technology. In simulations, the feasibility of this type of filter was demonstrated and reasonably good performance was obtained. The simulations show a center frequency tuning range from 6 GHz to 9.4 GHz and a noise figure of 8.8-10.4 dB depending on center frequency. Gain and Q-value are tunable in a wide range. Simulated IIP-3 and 1-dB compression point is -26 dBm and -34 dBm respectively, simulated at the center frequency 8.5 GHz and with 15 dB gain. Measurements on the fabricated device shows a center frequency tuning range from 6.6 GHz to 10 GHz, i.e. slightly higher center frequencies were measured than the simulated.

1 Introduction

The frontend of most wireless receivers needs a bandpass filter and a low noise amplifier. This is normally implemented as a combination of a LC-filter (external or integrated) together with an LNA. External LC-components have the benefit of high quality factors but they are extremely expensive to use. Integrated LC-components are preferred, but especially the inductors suffer from poor Q-values due to parasitics and only small inductances (< 10 nH) should even be considered to integrate [1]. It would be very attractive if the inductors could be avoided, as they are hard to integrate and use large chip area. Furthermore, it would be very attractive if the bandpass filter could be electronically tunable in both frequency and bandwidth. The present work is an attempt to design an active filter with these attractive properties. The goal of this design is not to demonstrate a final solution, rather the feasibility of this new approach.

2 Design theory

Active Recursive bandpass filters have recently become interesting for microwave applications [2, 3, 4]. A bandpass filter is accomplished according to the model in Fig. 1(a). This model is based on positive feedback where some of the output power is fed back to the input through a delay.



Figure 1: (a) Microwave model. (b) Block diagram.

cations, bandpass filters are aimed for replacing the combination of LNAs and resonator based filters, leading to smaller area and far increased tunability. Let us see how this principle of recursive filters can be applied to a standard BiCMOS process without using inductors, resonators, or transmission lines.

We propose a scheme according to Fig. 1(b), where the power combiner is replaced by an amplifier with two differential inputs. The necessary delay is replaced by the delays through the amplifier stages. Frequency tunability is achieved through variation of the delay, which can be studied through the amplifier time constant, τ . The delay through the amplifier chain corresponds to a phase shift ϕ_{delay} according

to $\phi_{delay} = \pi + 2\pi n = \omega_c \tau = 2\pi f_c \tau$. By connecting the positive/negative output to the negative/positive input, 180° low frequency phase shift is provided. Together with the delay through the amplifier chain, the necessary phase shift of 360° (and its multiples) is obtained. The multiples are strongly suppressed due to the limited bandwidth of the amplifiers. This implies $f_c = k/\tau$, where k is a positive integer. The proposed scheme in Fig. 1(b) can be viewed as a "nonoscillating ring oscillator" utilizing the same frequency tuning mechanism as used in VCOs based on ring oscillators [5]. The delay of each amplifier is proportional to its unity-gain frequency, $\tau = C_L/g_m$, where g_m is equal to I_C/V_T ($V_T = kT/q$) for bipolars. This means the time constant τ can be controlled by the bias current through each amplifier. The Q-value can be tunable through variation of the loop gain. The Q-value and gain are strongly correlated.

3 Circuit design

A fully differential design is chosen for its robustness and low sensitivity to supply noise [5]. The schematic for the recursive filter in Fig. 1(b) is shown in Fig. 2. The first stage should have two

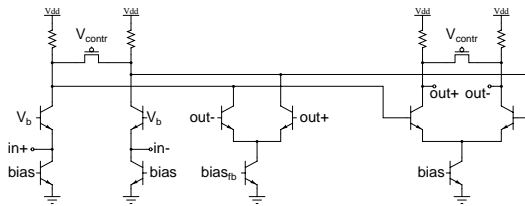


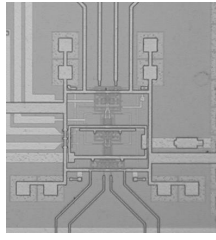
Figure 2: Transistor schematic.

differential inputs, which is achieved by connecting two differential pairs in parallel with the same load resistors. The differential input signal is fed to a common-base stage having an input impedance $r_e = \alpha/g_m \approx 1/g_m = 50 \Omega$. Malmqvist found that minimum noise figure was obtained by having maximum coupling coefficient for the input signal (α close to 1 in Fig. 1(a)) [4]. We choose to make the feedback input transistor 1/4 as large as the input transistor to get a coupling ratio of 4 for the input signal (only true when the two transistors have the same current density). The ratio of the g_m (the coupling factor), between the input and feedback transistor will change with center frequency tuning. The second stage in Fig. 1(b) and Fig. 2 is a simple differential amplifier. The bias current through the input transistors and the second stage is fixed. The reason for having a fix bias current through the input transistors is to keep the impedance matching. The input called *biasfb* is used for controlling the loop delay and hence for frequency tuning. The delay should be proportional to the current (*biasfb*) in the feedback stage. But, because of fundamental properties of bipolar transistors, f_T depends on the current density and the relation between center frequency and bias current is not strictly proportional. The gain is controlled by PMOS transistors connected across the differential outputs. The gain can thus be tuned by the voltage V_{contr} connected to these PMOS devices in Fig. 2. Unfortunately, the gain control is not independent of the delay control since a change of bias current in the feedback part also change the DC-point in the input stage. A small change in gain will also be due to the change in g_m for the feedback transistors when the bias current is changed. The output buffers are not shown in Fig. 2, but are implemented as simple common-collector stages. The common-collector stages are designed for an output impedance of 50Ω .

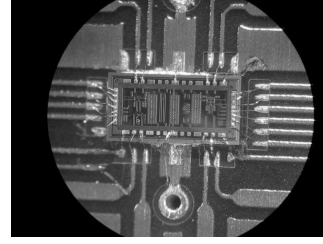
4 Simulation and measurement results

The recursive filter previously described was fabricated in a $0.35 \mu\text{m}$ SiGe BiCMOS process having a supply voltage of 3.3 V and maximum f_T of 45 GHz. A chip photo of the active recursive filter is shown in Fig. 3(a). The picture in Fig. 3(a) corresponds to a size of $400 \times 450 \mu\text{m}^2$ and the active circuit has a size less than $200 \times 200 \mu\text{m}^2$. In Fig. 4 we see the die mounted directly onto a PCB (recursive filter to the right). DC-biasing was bonded onto the PCB while RF probes were used for input and output signals.

Simulations of the circuit showed a center frequency tuning range of at least 6-9.4 GHz. Fig. 4 shows the simulated transfer characteristics when the filter was tuned to a center frequency of 6.8, 8, and



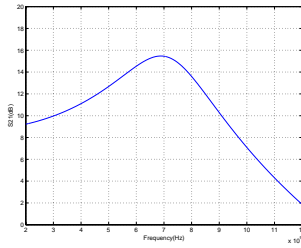
(a)



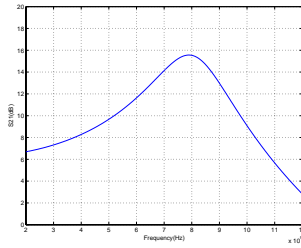
(b)

Figure 3: (a) Chip photo of the active recursive filter. (b) Chip mounted onto the PCB.

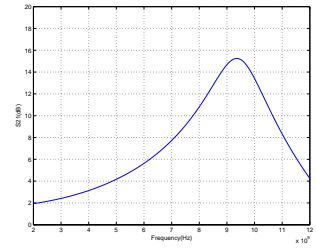
9.4 GHz, respectively, in all three cases S_{21} was set to 15 dB. The corresponding power consumption (including bias circuitry and buffers) was simulated to 19.4, 20.4, and 25.2 mW, respectively. The noise figure for the three center frequencies above is 8.8, 9.3, and 10.4 dB. Lower noise figures can be accomplished by designing, mainly the input stage, for a lower noise figure. However this will be at the expense of the power consumption. The Q-value for the three different cases shown in Fig. 4, where the gain is



(a)



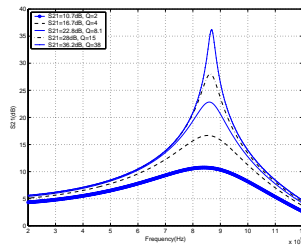
(b)



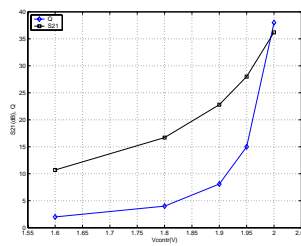
(c)

Figure 4: S_{21} , center frequency tuned to (a) 6.8 GHz, (b) 8 GHz, and (c) 9.4 GHz.

about 15 dB are 2, 2.9, and 5 respectively. By raising the gain control voltage, V_{contr} in Fig. 2, the gain and Q-value is increased, while leaving the center frequency essentially unaffected. Fig. 5(a) shows five different curves with the same center frequency, 8.5 GHz, but different gain and Q-values. Fig. 5(b) shows gain and Q-value versus control voltage. Fig. 5 shows a possible tuning range of the gain from at least 10.7 dB to 36.2 dB and a corresponding Q-value of 2 to 38. To evaluate the large signal behavior the 1-dB compression point and the third order intercept point was simulated. The input referred 1-dB compression point was recorded to be -34 dBm, at a center frequency of 8.5 GHz and a power gain of



(a)



(b)

Figure 5: (a) Different gain and Q-values simulated at 8.5 GHz center frequency. (b) Q-value and gain vs. control voltage.

15.1 dB. IIP-3 was simulated using two tones at 8.5 GHz and 8.6 GHz and the result was -26 dBm.

Due to the lack of proper measurement equipment for noise figure and linearity measurements at these frequencies only S-parameters have been measured. Differential RF probes together with 0/180° hybrids were used for creating a differential input signal and to transform the differential output back to the single ended input of the network analyzer. Fig. 6 shows both the measured and a polynomial fitted curve of the measured one. The jagged nature of the measured curve is due to mismatches in the measurement setup and the fact that S22 was worse than expected. The center frequency showed a tuning range of at least 6.5-10 GHz. Fig. 6 shows the power gain at the three different center frequencies 6.5, 8.6, and 10 GHz. The measured and simulated performance seems to agree quite well.

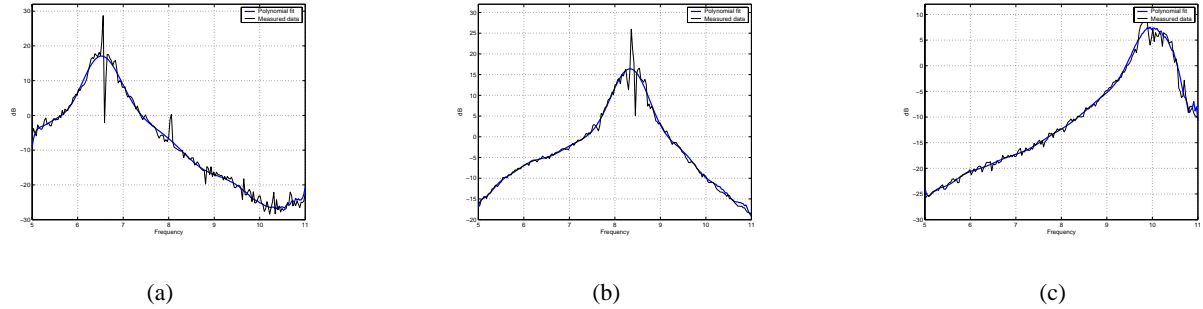


Figure 6: S21, center frequency tuned to (a) 6.5 GHz, (b) 8.3 GHz, and (d) 10 GHz.

5 Discussion and Conclusion

A new form of bandpass filter, based on the principle of recursive filters, was proposed and implemented in 0.35 μm BiCMOS. Simulations and measurements have shown that this approach is feasible, at least for applications with not too high demands regarding linearity and noise. However, both noise and linearity should be possible to improve by taking that into account when redesigning the proposed circuit.

The frequency tuning range is very wide and extends from 6.5 to 10 GHz. Moreover, the Q-value and gain of the device is tunable in a broad range and high Q-values can be achieved. The simulated noise figure is 8.8-10.4 dB depending on center frequency. The input referred 1-dB compression point and IIP-3 was simulated and recorded to -34.0 dBm and -26.0 dBm, respectively when the gain was tuned to 15.1 dB. The power consumption of less than 25.2 mW, including bias and output buffers, must be considered low for an active filter at these frequencies. If the recursive filter is designed with a better noise figure and linearity it could successfully be used as a tunable low noise amplifier. With high enough Q-value such an LNA could be used without an external filter between antenna and LNA.

In conclusion, we have demonstrated the feasibility and benefits of a low power, inductorless, active recursive filter in BiCMOS, useful at least in less demanding applications.

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