A comparison of topology and technology of balanced VCOs intended for use in a 60 GHz WLAN system

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ABSTRACT— **We present a comparison of balanced Colpitt and Negative g_m oscillators in a GaAs pHEMT process as well as comparison with similar designs in a SiGe BiCMOS process. We believe that this comparison will give more insight into drawbacks and advantages of the two topologies and topologies. The comparison between GaAs pHEMT versus SiGe HBTs show that pHEMT oscillators also are capable of producing low phase noise comparable with SiGe HBT oscillators. All oscillators are fully integrated with on-chip resonators and have mainly been designed with focus on low phase noise**.

I. Introduction

Millimeter-wave wireless communication systems are promising candidates to meet the demands of future ultra wideband wireless system. Especially 60 GHz system is watched with keen interest due to its high information capacity and small co-channel interference due to large oxygen absorption. It is also important to get low power consumption, small size, high integration to necessitate widespread use and low cost. For microwave circuits GaAs pHEMTs has been the main technology and to some extent also III-V HBT processes. Since most other circuits, like LNAs, mixers, PAs, in the system are readily made in pHEMT technology [1] it is interesting to implement also the VCO using pHEMTs here to make design and fabrication more cost effective.

The system architecture we're focusing on has the VCO at 7.5 GHz and a multiplier chain up to 60 GHz. This makes the phase locking of the VCO in a PLL easier since PLLs exists commercially and are also easier to implement at 7.5 GHz.

We present the two topologies in section II, Negative g_m in IIa and balanced Colpitt in IIb. The technologies, GaAs pHEMT and SiGe HBT are presented in section III.

One of the limiting factors in an integrated VCO is the lack of high-Q varactors. This is being addressed in section IV there we present the use of the pHEMTs $C_{gs}//C_{ds}$ as variable capacitances. A comparison and conclusion is presented in section V and VI.

II. Topologies

All investigated oscillators are balanced to reduce phase noise and to supply differential signal.

A. Negative g_m

In this topology the cross-coupled pair will supply a negative resistance, $R_{in} \approx -2/g_m$ seen from the tank, which cancel out the losses in the tank, thus fulfilling condition for oscillation. A capacitive divider consisting of the capacitors C_1 and C_2 is also incorporated between the negative resistance part and the tank to reduce loading of the tank as well as block the gate/base DC-bias.

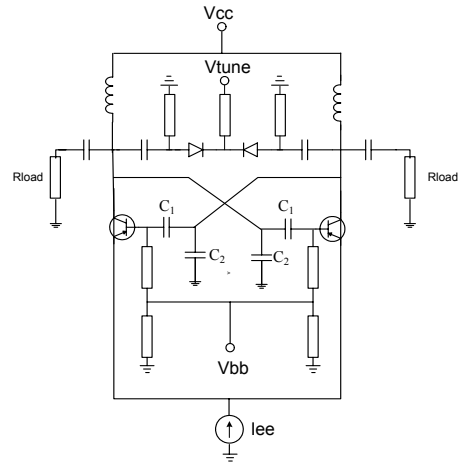

Fig. 1. Negative g_m oscillator topology. Same for HEMT, but with other source loading.

B. Balanced Colpitt

In this topology the tank is loaded through a capacitive divider C_1, C_2 . The ratio C_1/ C_2 is a critical parameter for low phase noise a value around 1/3 is usually a good starting guess.

In both cases no output buffer is realized. In the pHEMT design we use an inductor RF block for the varactor control voltage in order to reduce the noise. In the SiGe case HIPO-resistors were used since inductors were too bulky in the design, see Figure 5 for chip photo.

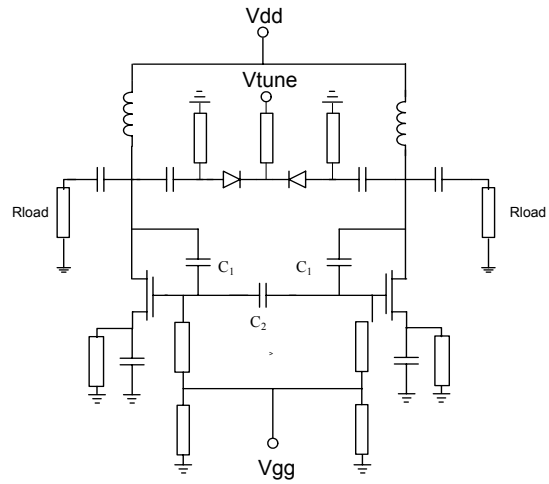

Fig. 2. Colpitt oscillator topology. Same for HBTs but with other emitter loadings

III. Technologies

The GaAs pHEMT process is a 0.14 μm gate length process with double delta doped layer structure utilizing high drain current density with high breakdown voltage, with measured f_t and f_{max} of 100 GHz and 180 GHz respectively.

The SiGe HBT process is STMicroelectronics BiCMOS7 process [2]with 0.25 μm emitter width process with 5 metal layers with measured f_t and f_{max} of 70 GHz and 90 GHz respectively.

IV. Varactor

The ordinary varactor diode in the pHEMT process has a varactor length of 3 μm. This yields a considerably high series resistance than the 0.14 μm gate length of a pHEMT. We therefore utilize $C_{gs}//C_{gd}$ in a pHEMT with connected drain and source terminal. The drawback is that the capacitance per μm-varactor width is lower. In order to get a high enough capacitance value and better tuning ratio we have parallel-coupled a large number, ~20, of wide, ~60 μm, fingers. This yields a relative high-Q varactors with acceptable tuning range, see Figure 3. It can be found from this that the tuning ratio is about 2.5 with a Q-value ranging from 23 to 51.

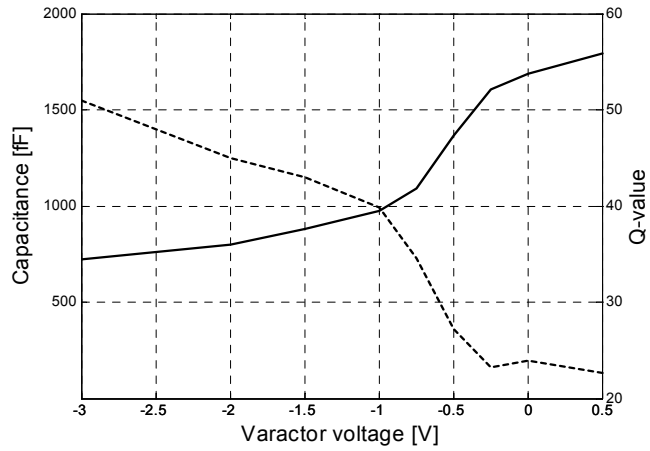

Fig. 3. Capacitance(-) and Q-value(--) at 7.5 GHz for pHEMT varactor used in pHEMT VCOs.

The varactor in the SiGe HBT VCO there a P+/N well structures specially designed for low losses. Tests with a similar approach as for the pHEMTs using nmos-tranistor's $C_{gs}//C_{gd}$ as variable capacitor have been carried out but it turned out that the optimized P+/N-well varactors had better performance. The fabrication of sufficiently large nmos-devices also incorporated risk of ESD damage during processing.

V. Comparison

The performance of the different designs is summarized in table 1. The normalized figure of merit, FOM, suggested by Klinget [3] is one of the better suggested so far.

$$FOM = 10\log\left(\left(\frac{f_{center}}{\Delta f}\right)^2 \frac{1}{L(\Delta f)\cdot V_{dd} I}\right)$$

Where f_{center} is oscillation frequency, Δf offset at which phase noise, $L(\Delta f)$ is measured, Vdd is bias voltage and I is the current in the oscillator.

TABLE I.
Comparison of the different VCOs.

Ref.	Technology	Topology	£@100 kHz offset [dBc/Hz]	F_{center} [GHz]	FOM
This work	0.15 um pHEMT	Neg. g_m	-89	7	198.6
This work	0.15 um pHEMT	Colpitt	-95	7.5	201.1
[4]	0.15 um pHEMT	Neg. Resistance	-68	28	188.3
This work	0.25 um SiGe HBT	Neg. g_m	-92	4.5	194.5
[5]	0.35 um SiGe HBT	Neg. g_m	-98	5	210.2

We have also included some relevant work of others [4],[5] as comparison. It can be seen that our pHEMT VCOs are approaching the performance of SiGe HBT based VCOs. The flicker noise of the pHEMT is substantially higher than the SiGe HBTs but it is believed that the up conversion of noise is worse for HBTs than for HEMTs [6],[7].

The inductors in an III-V technology can also be made with higher Q since we have a thick gold metal with low resistivity and high conductivity instead of Aluminium. As well as a high resistivity substrate, GaAs compared to low resistivity SiO_2- and Si–substrate in BiCMOS processes. Even though the inductors in the BiCMOS process were made in the thicker metal 5 layers with polysilicon shielding to minimize substrate losses.

Both the Colpitt and negative g_m VCOs show good noise performance so the choice of topology is more of a layout issue.

Die photos of the Colpitt VCO in GaAs pHEMT technology and the negative g_m VCO in BiCMOS is found in Figure 4 and 5.

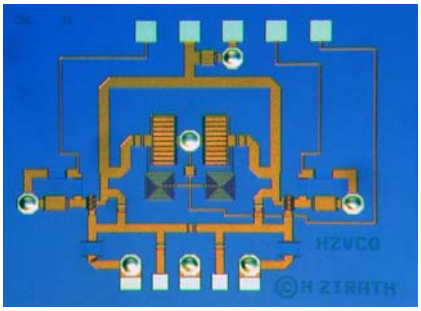

Fig. 4. Die photo of Colpitt oscillator in a GaAs pHEMT technology.

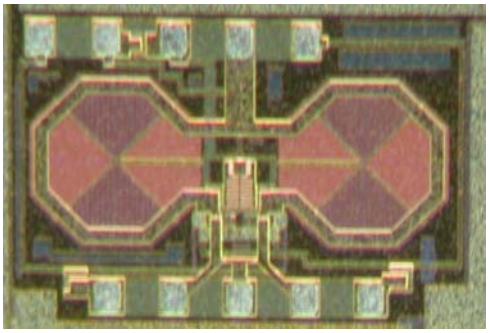

Fig. 5. Die photo of negative g_m oscillator in a SiGe HBT, BiCMOS technology.

VI. Conclusions

We have shown that VCOs can be made with good phase noise performance in a GaAs pHEMT technology to some extent comparable with SiGe HBTs. The reason for the low phase noise performance is due to the high-Q obtained from HEMT-varactors as well as higher Q-value of inductive parts. It is also believed that the low frequency noise in the transistors is more severely up converted in HBTs than HEMTs.

VII. Acknowledgement

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