

## A SIGE 24 GHZ ZERO-IF DOWNCONVERTER

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### SUMMARY

This paper describes the design of the main building blocks of a 24 GHz zero-IF downconverter: a voltage controlled oscillator (VCO) and a sub-harmonic mixer (SHM). The circuits have been monolithically implemented in a SiGe HBT process production line using low-resistivity ( $20\Omega\text{cm}$ ) substrate. Measured results are presented, showing the feasibility of direct conversion receiver (DCR) implementations for the 24 GHz ISM band using a low-cost standard process.

### INTRODUCTION

The direct conversion (or zero-IF) receiver (DCR) is currently experiencing a come back in terms of popularity among RF front end designers and is more and more considered as a viable alternative to standard super-heterodyne architectures. Today it is implemented in GSM mobile terminals from all major manufacturers and several semiconductor companies are currently developing DCR implementations for WCDMA and CDMA [1]. A complete DCR for 5-6 GHz is described in [2] and provides the foundation for the work presented in this paper. To the authors' knowledge, no DCR has so far been implemented in the 24 GHz ISM band.

The motivation for using DCR:s as opposed to super-heterodynes – e.g. lower complexity, higher integrability, lower power consumption – as well as the key implementation challenges – LO self-mixing, second-order non-linearity, 1/f noise – is thoroughly examined in [3]. The approach taken in this paper to solve some of the implementation challenges is

- 1) use a differential VCO, ideally avoiding any second-order non-linearity and
- 2) use a sub-harmonic mixer, ideally avoiding any LO self-mixing (i.e. LO signals injected in the RF path of the mixer causing a DC offset) since the LO and RF frequencies are well separated.

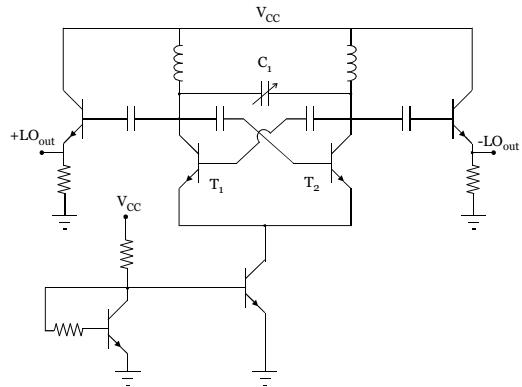
Presented in this paper are two circuits, a VCO and a SHM, which put together constitutes a downconverter for a DCR in the 24 GHz ISM band.

## VCO Design and Results

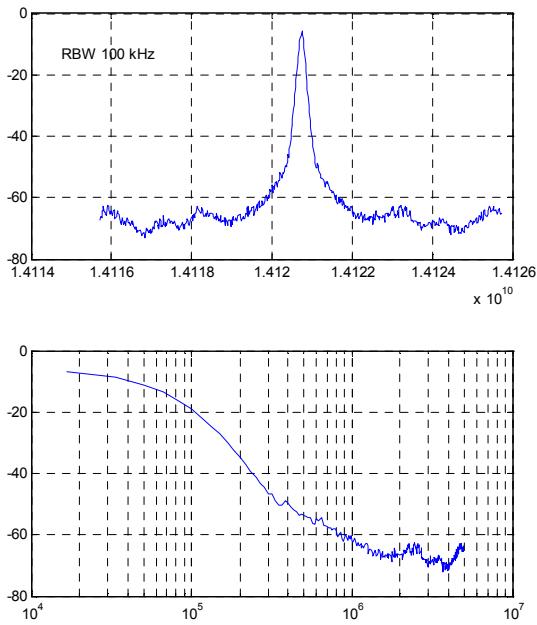
Fig. 1 shows a simplified schematic of the VCO. It consists of an on-chip LC-tank and a cross-coupled pair of transistors, T<sub>1</sub> and T<sub>2</sub>, which compensates for the losses in the tank. The tank inductances are implemented as standard circular spiral inductors, each 0.25 nH, connected to V<sub>CC</sub> at the virtual ac ground point in the symmetry plane. The short interconnects between the transistors and spirals add some inductance that partly compensates for the negative mutual inductance of the spiral pair.

The capacitance is provided partly by the parasitic base-collector capacitance of the amplifying transistors and partly by a varactor. The varactor is realized by reverse biasing the emitter-base junction of a number of NPN-transistors connected in parallel (for maximum Q due to reduction of base resistance) making the depletion zone acting as a tunable capacitor. To further increase the circuit Q-value, two series (for symmetry reasons) capacitors are connected in parallel with the varactor. These are not shown in Fig. 1. The output of the VCO core is connected to buffer amplifiers (emitter-followers) through small capacitors to reduce oscillator frequency pulling.

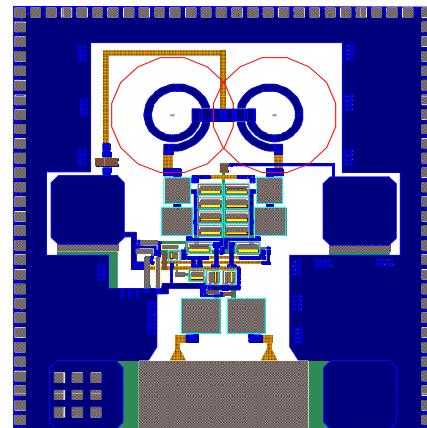
Measured output power is in excess of +2 dBm over the entire oscillating frequency range of 14.12–14.56 GHz, which is more than enough to drive the LO sections of the mixer. Measured phase noise is approximately –95 dBc@1MHz offset at maximum reverse bias, slightly lower for lower frequencies.



**Figure 1 - Simplified schematic of VCO**



**Figure 2 - Spectral output and phase noise of VCO**



**Figure 3 - Layout of VCO**

## SUB-HARMONIC MIXER Design and Results

Fig. 4. shows a simplified schematic of the sub-harmonic x2 mixer. The SHM is a modified Gilbert cell [4] with two stacked LO switching stages (transistor quads) driven by quadrature phase (I/Q) local oscillator signals resulting in mixing action at twice the LO frequency. This reduces DC offset problems in direct conversion receivers since LO self-mixing is avoided. Integrated in the SHM is a one-pole polyphase filter prior to the LO inputs, producing the necessary phases from a differential input. The IF output is buffered by emitter followers to facilitate low impedance loading. In a real life application these buffers could be replaced by OP-amplifiers. This implementation lacks the standard RF-stage (or gain-stage) since the mixer was designed for validation of the mixer core at high frequencies (24 GHz). This results in a lower gain and higher impedance mismatch (more reflected power) at the RF-input compared to the case with the RF-stage included.

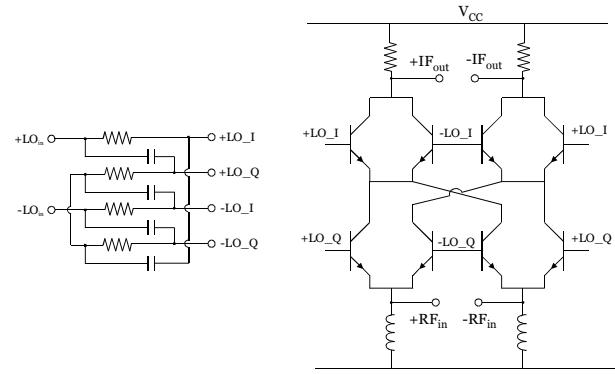


Figure 4 - Simplified schematic of SHM

The IF output was connected to a high impedance oscilloscope during measurements. For an RF-input of  $-19.2 \text{ dBm}$  (minus reflection) at 24 GHz, an output voltage of 28 mV was measured at 50 kHz with an LO frequency of 12 GHz and sufficient LO voltage swing to fully switch the LO transistors on and off (approximately 100mV). Should this voltage be applied to the standard  $50 \Omega$  load, this translates to an output power of  $-21 \text{ dBm}$ . Taking reflections at the RF input port into account the conversion gain of the mixer core is approximately  $0 \text{ dBm}$ , which with the inclusion of an RF-section and impedance matching should result in a fairly high conversion gain (approximately  $+10 \text{ dB}$ ).

Fig. 5. shows the layout of the SHM, with the RF input at the bottom, LO input at the top and IF output at the right side.

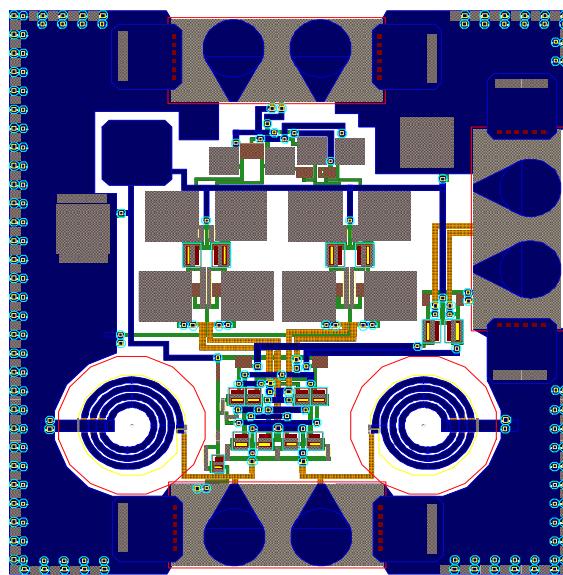


Figure 5 - Layout of the SHM

## **DISCUSSION**

The circuits have been implemented and measured with good results. Unfortunately the VCO oscillated at an elevated frequency, probably due to the mutual negative inductance of the spirals lowering the total positive reactance and thus raising the frequency. As a consequence, system performance could not be measured. A VCO with corrected inductances are currently in fabrication as well as the complete downconverter (VCO+SHM) and will be published in a near future.

## **CONCLUSIONS**

A VCO and a SHM for a 24 GHz direct conversion downconverter has been designed and measured. Results indicate that sub-harmonic mixing is feasible at high frequencies using a standard production line SiGe process.

## **ACKNOWLEDGEMENT**

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