

4H-SiC MOSFETs WITH N₂O GROWN GATE OXIDE

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ABSTRACT

We report on processing and characterization of lateral n-channel 4H-SiC MOSFETs. We find that growing the gate oxide in nitrous oxide (N₂O) ambient results in a significant enhancement of the electron inversion channel mobility. The peak field effect mobility varies between 30 and 90 cm²/Vs in these normally off devices while transistors with a conventional wet or dry gate oxide exhibit mobilities ranging between 1-10 cm²/Vs. The mobility enhancement is correlated with a significant reduction of the density of shallow interface states with energies close to the SiC conduction band edge. This is revealed from capacitance-voltage (C-V) data and thermally stimulated current measurements (TSC). Furthermore, we find that the ohmic contact annealing results in an increase in the density of interface states which most likely results in a reduction of the inversion channel mobility.

INTRODUCTION

The great potential of silicon carbide 4H-MOSFET devices for high frequency and high power applications has thus far been hampered by unacceptably low electron inversion channel mobilities typically in the range of 10-40 cm²/Vs. The low mobility is attributed to high density of interface states near the SiC conduction band edge resulting in charge trapping and Coulomb scattering at the interface. Several approaches have been used to increase the inversion channel mobility. One of the methods is to grow or post-anneal the gate oxide in nitric oxide (NO) or nitrous oxide (N₂O). Such oxide/SiC structures contain lower density of the detrimental interface states than conventionally grown oxides. MOSFETs with NO grown oxides with peak field effect mobilities up to 48 cm²/Vs have been reported as well as transistors using N₂O grown oxides with mobilities up to about 25 cm²/Vs [1-3]. In both cases nitrogen is observed to accumulate at the interface and is believed to passivate (or dissolve) defects at the interface. In this work we report on 4H-SiC MOSFET normally off devices with N₂O grown gate oxides which exhibit field effect inversion channel mobilities as high as 90 cm²/Vs.

EXPERIMENTAL

The MOSFETs are made on commercial p⁺ substrates with a 10 micron thick p-type epilayer with doping concentration of 5x10¹⁵ cm⁻³. The source and drain regions are made by five subsequent phosphorus ion implantations at 650 °C followed by implant activation anneal for 10 min at 1600 °C in argon/silane mixture. The gate oxides were grown in N₂O ambient at a temperature of 1220 °C. The oxidation time was chosen to result in oxide thicknesses between 50 and 200 nm. The oxide thickness was estimated from capacitance-voltage (C-V) data and a profile meter. Reference gate oxides were made by wet oxidation at 1100 °C for 400 min followed by densification anneal in Ar at 1100 °C for 60 min. The thickness of the reference oxides was about 70 nm. Ni was evaporated and annealed in rapid thermal processing unit for 5 min in Ar at 1000 °C to form the source and drain contacts. Evaporated Ti-Au layer was used as a gate metal and Al as a backside contact. The gate length of the transistors varies between 2 and 100 μm and the gate width is 1 mm. In addition n- and p-type reference MOS capacitors were fabricated to examine the SiO₂/SiC interface.

RESULTS AND DISCUSSION

Fig. 1 shows typical output characteristics of a MOSFET with a gate oxide grown in N_2O . The threshold voltage is approximately 3 V and the peak field effect mobility is $40 \text{ cm}^2/\text{Vs}$. The field effect mobility for devices with different channel lengths, located adjacent to each other on the wafer, is depicted in Fig. 2. As seen, the mobility does not depend significantly on the channel length. In general the mobility of the transistors with N_2O grown oxides varies between 30 and $90 \text{ cm}^2/\text{Vs}$ with the average value of $40 \text{ cm}^2/\text{Vs}$. We have also estimated the field effect mobility by AC measurements of the transconductance both in the linear and the saturation region of the transistors. This data agrees with the mobility values obtained from the DC characteristics and we see no frequency dependence of the field effect mobility within the interval 10 Hz -1 MHz.

In Table 1 we compare the field effect electron channel mobility extracted from the transfer characteristics for transistors with differently prepared gate oxides. We obtain the highest mobility using N_2O grown oxides while wet oxide post-annealed in N_2O at $1220 \text{ }^\circ\text{C}$ gives mobility of about $5 \text{ cm}^2/\text{Vs}$. A wet reference oxide gives mobility of about $2 \text{ cm}^2/\text{Vs}$. These results are in accordance with previous studies except the mobility for our N_2O grown oxides is somewhat higher than previously reported [3]. However, in order to make a direct comparison possible the Hall mobility should be extracted instead of the field effect mobility.

The mobility enhancement is correlated with a significant reduction of the density of shallow interface states with energies close to the SiC conduction band edge. This is revealed from C-V data and thermally stimulated current measurements (TSC) on n-type reference capacitors. Fig. 3 shows the frequency dispersion in the C-V curves for the N_2O grown MOS structures and wet oxide reference capacitor. The dispersion near accumulation is much smaller in the N_2O sample which shows that the number of shallow interface states is reduced as compared to the wet oxide. This is further revealed in Fig. 4 which shows the interface state density for both oxides extracted from the data in Fig. 3. The interface state density in the wet oxide is more than two times higher than in the N_2O grown oxide for the whole energy range.

Oxide	Average μ_{FE} [cm^2/Vs]	Best μ_{FE} [cm^2/Vs]
N_2O grown	40	90
wet + N_2O anneal	5	15
wet	2	10

Table 1. Field effect mobility in transistors with differently prepared gate oxides.

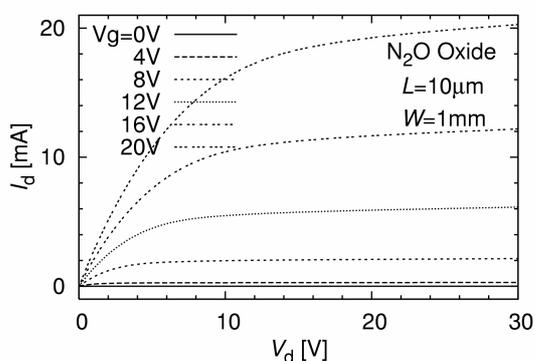


Fig.1: Output characteristics of a transistor with oxide grown in N_2O .

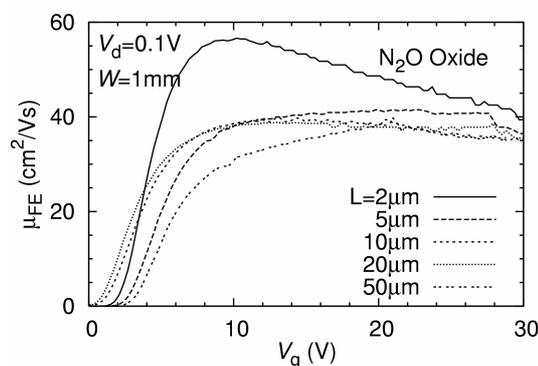


Fig. 2: Comparison of the field effect electron channel mobility in transistors with different gate lengths.

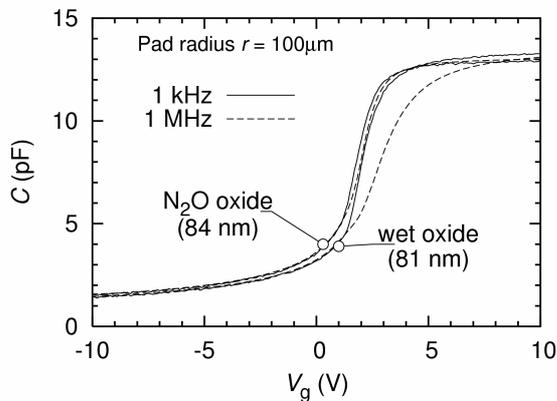


Fig.3: C-V data of a N_2O grown n-type MOS structure and wet oxide reference capacitor.

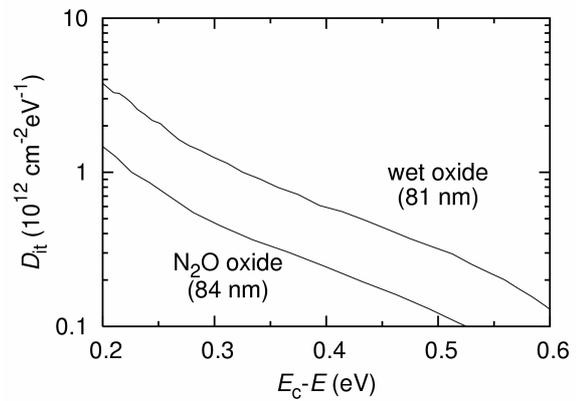


Fig. 4: Interface state density extracted from the C-V data in Fig. 3.

It is also possible to obtain an estimate of the interface state density by thermally stimulated current analysis (TSC). In the TSC technique the MOS structure is accumulated at a voltage V_a and the sample is cooled to low temperature. Thereafter the voltage is switched to depletion and the temperature is ramped up to room temperature. During the ramp-up period a current due to electron emission from interface states to the SiC conduction band is observed [4,5]. Typical TSC spectra for a reference wet oxide and for an N_2O grown oxide are shown in Figs. 5 and 6. The peak at ~ 110 K and the hump at ~ 80 K correspond to two types of traps found in all oxides so far investigated on off axis Si face substrates [5]. Both traps are present in the N_2O grown sample but their density is much smaller than in the wet oxide sample. The spectra are taken for increasing accumulation voltages as indicated by the arrow. The signal increase with accumulation voltage is due to more trapping of electrons in interface states. In the wet oxide sample the signal does not saturate and we have evidently not filled all the interface states available. In contrast, in the N_2O sample the signal saturates at high accumulation voltage which means that virtually all the interface states are occupied. The area underneath the curves is a measure of the total charge trapped in these interface states and this is shown as the inset in Fig. 6 as a function of the electric field across the oxide.

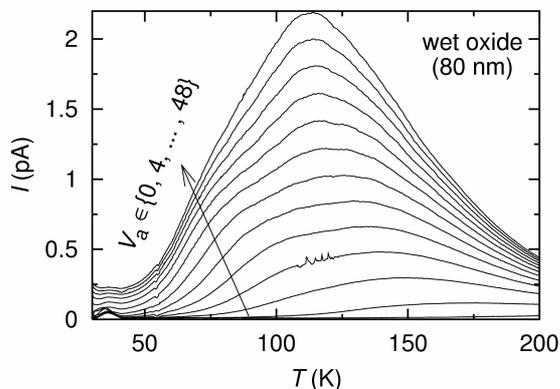


Fig.5: TSC spectra of a wet oxide n-type reference capacitor. The pad radius is $150 \mu\text{m}$. The heating rate was 12 K/s .

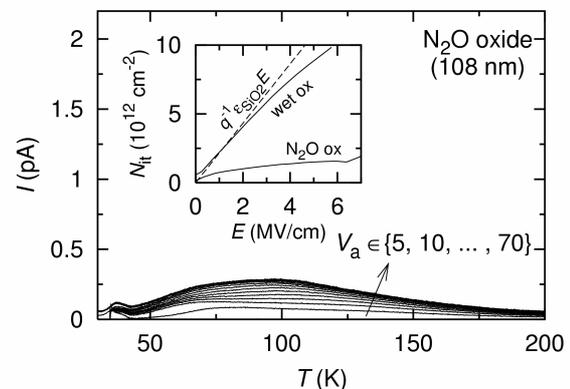


Fig.6: TSC spectra of an N_2O grown oxide n-type capacitor. The inset shows the charge trapped in interface states as a function of the electric field across the oxide for wet oxide and N_2O grown oxide. The broken line in the inset marks the total charge in the capacitors.

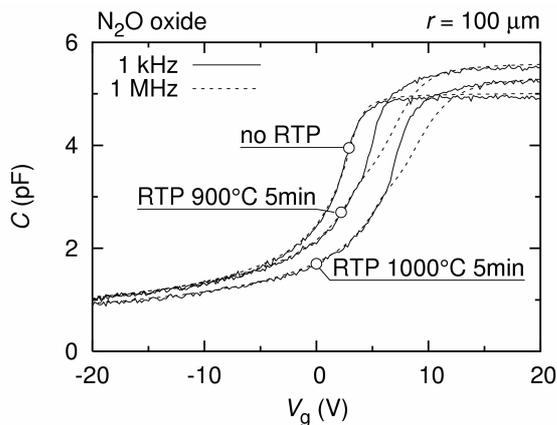


Fig.7: C-V data of a N₂O grown MOS structures on n-type 4H-SiC substrate showing the effect of RTP contact anneal.

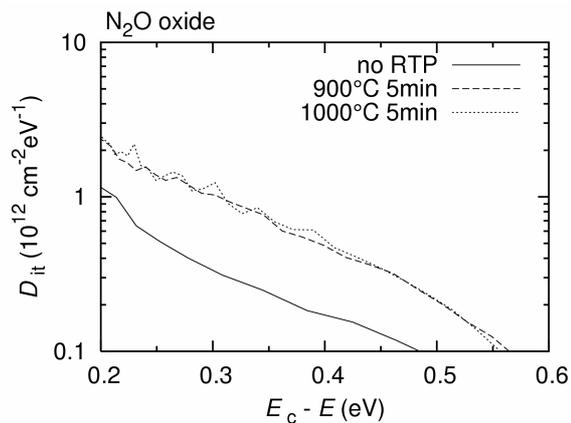


Fig. 8: Interface state density extracted from the C-V data in Fig. 7.

It is unclear if the use of N₂O during oxide growth results in a passivation of these interface states or if they are not as easily formed in N₂O ambient. We have experienced that postoxidation anneal after growth in N₂O can result in an increase of the density of these interface states. In particular, we note the sensitivity of the interface to the rapid thermal processing step used to form the nickel-silicide ohmic contacts. An example of such a study is depicted in Figs. 7 and 8. In Fig. 7 we compare the C-V curves for MOS capacitors with and without an RTP anneal. After oxidation in N₂O the sample was annealed in RTP as indicated and thereafter Al contact was made by evaporation to finalize the MOS structure. We note that the RTP has a negative effect on the interface quality. The frequency dispersion increases and the flatband voltage shifts to the right suggesting increased electron trapping in interface states. This is revealed in Fig. 8 which shows the interface state density extracted from the data in Fig. 7. The interface state density increases after RTP anneal but is still lower than the interface state density in wet reference oxides (see Fig. 4.). We expect to see a significant increase in the field effect mobility if the ohmic contacts can be made without affecting the interface state density.

ACKNOWLEDGEMENTS

We thank Dr. Christer Hallin at Linköping University, Linköping, Sweden for the implant activation. This work was financially supported by Philips Semiconductors, Nijmegen, The Netherlands.

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