Design and characterization of a broadband SiC power amplifier

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Due to the proximity of military and civilian bands at the relevant frequencies low frequency radar and EW systems needs amplifiers which combine a broadband coverage, a high output power and efficiency with a good linearity. The wide bandgap semiconductors SiC and GaN offer an impressive RF and microwave power-frequency capability [1] but relatively few SiC transistor amplifiers have been designed for frequencies below 500 MHz. Recently, however, F Villard et al. described a SiC MESFET with an output power of 37,5 W, a gain of 8 dB, an efficiency in class AA-B of 55% at 500MHz [2]. The IMD3 level with 10-dB back-off from the 1 dB compression point and a 1 MHz frequency offset between tones was – 35dB. Using 10W Lateral Epitaxy SiC MESFET power transistors fabricated at AMDS AB we have done a preliminary design and characterization of a wideband 100 – 500 MHz SiC-based power amplifier. The amplifier is designed for a broadband multifunction EW system.

AMDS POWER TRANSISTORS

The advantage of SiC for the manufacture of high frequency power devices is derived from the ability to operate at high voltage levels and hence high impedance while maintaining high frequency capability. The realisation of this advantage has so far been limited due to "punch through" or so-called short channel effects in which the high applied drain voltage limits the ability of the gate to control the channel. The voltage limitation of the standard MESFET design has been extended using a novel design which combines concepts typically used in Si LDMOS technology [3]. The key component of the AMDS MESFET design (the so called LE MESFET) is the buried depletion stopper underneath the active channel, as it is shown in Figure 1. It blocks the penetration of high electric fields underneath the channel and can also minimize the electric field concentration at the drain-side edge of the gate. Since it also decreases the non-linear drain-to-gate feedback capacitance it might also improve the device linearity at high power levels. Devices have been fabricated using both Okmetic and CREE substrates but with no significant difference in performance.

A high-resistivity p^0 buffer layer was deposited, which had a doping of around 1×10^{15} cm^{-3} or lower. This buffer is used to provide some spacing between the drift region and the semi-insulating substrate and therefore suppress any effect of deep-level traps or extended defects in the substrate [4]. Epitaxial deposition was made using a low-pressure hot-wall CVD technique at 1600°C. Trenches are then plasma etched into the buffer layer. The trench configuration corresponds to the desired layout of the source regions. The source stack employed consists of an Al-doped p-type depletion stopper and a nitrogen-doped n-type source. The doping of both p-type and n-type layers was around 1×10^{20} cm^{-3}. It should be noted that thickness and doping for the sidewall epitaxy are generally not identical to those for the normal epitaxial growth.

A standard planarization technique using silicon dioxide as a masking layer is used to first fill the trenches, the crystals are then plasma etched to remove the highly doped layers in unmasked regions. The active layer is then subsequently epitaxially grown by CVD. The active layer doping and thickness is around 3×10^{17} cm^{-3} and 0.26-0.29 µm respectively. Source and drain contact layers were formed by nitrogen ion implantation to a dopant concentration of around $2\text{-}6\times10^{19}$ cm^{-3} with subsequent activation anneal. No attempts to form a dedicated contact region to the p^+ depletion stopper have been done in this study, with an expectation for a tunnel contact between n^{++} and p^{++} regions. Ohmic contacts to source and drain are formed by sintering nickel. The gates are 0.4 µm long and are patterned using electron beam lithography and lift off. The gate stack employed is Ti/Pt/Au. The device layout includes a total gate width of 4.6 mm.

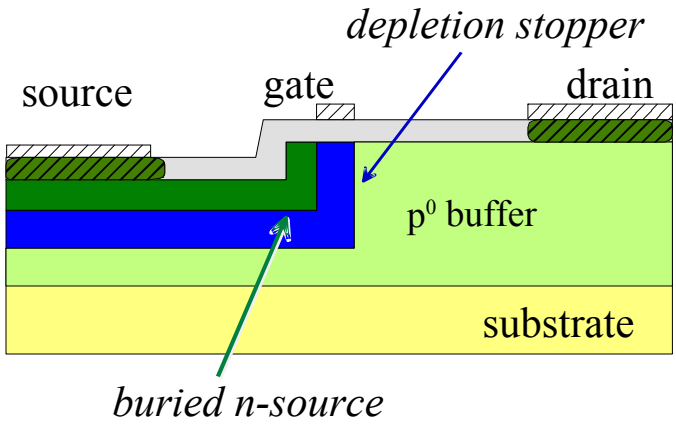

Figure 1. Cross-section of a silicon carbide MESFET.

AMPLIFIER DESIGN

Due to lack of load-pull measurements at the relevant frequencies the design of matching networks for the amplifier was mainly based on small signal S-parameter measurements made on the packaged transistor. The matching and bias networks shown in fig. 2 were realized using lumped circuits on 0.508 mm thick Rogers Duroid 5880. The lossy components in the RF parts of the matching networks where, in this preliminary design, included to ensure stability at all frequencies.

The physical size of the amplifier is 22×53 mm. The transistor was mounted on an open 1 mm thick CuMoCu flange carrier which in turn was attached to an aluminium heat sink that was held at 14-17 °C during the measurements.

The primary design objectives were to achieve a gain above 15 dB, a reasonable output reflection coefficient and stability.

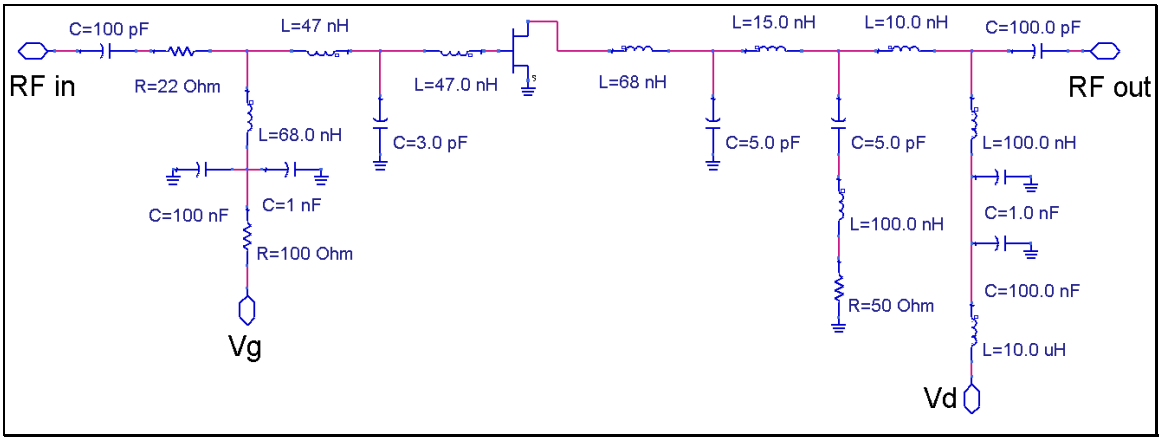

Figure 2. Schematic of the matching and bias networks.

The measured small signal gain flatness was within 9 dB across the band. It should be noted that the transistor S-parameters used in the simulation were measured on a different (but similar) transistor than the one used in the measured amplifier.

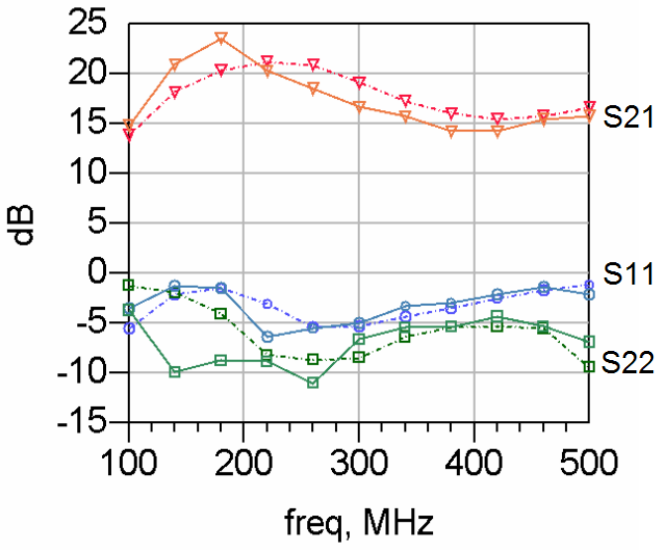

Figure 3. Simulated (dash-dotted) and measured (solid) small signal S-parameters of the amplifier at V_d = 50 V and V_g = -15 V

Power measurements were carried out between 100 MHz and 500 MHz with 100 MHz intervals. All measurements were made with a drain bias of 50 V. The 1 dB compression point was reached at an output power around 37 dBm except at 500 MHz where only 33 dBm was measured. The maximum output power measured was 39.6 dBm at 300 MHz corresponding to a power density of 2 W/mm of gate periphery. Figure 4 shows the measured gain and power added efficiency (PAE) at 300 MHz as a function of output power for two different gate bias settings. One bias point (V_g = - 5 V, I_{dq} = 130 mA) is close to class B conditions while the other (V_g = -12 V, I_{dq} = 350 mA) is closer to class A conditions. As can be seen in figure 4 the 1 dB compression point (P_{1dB}) is at an output power of 37 dBm for both bias points while the gain is slightly better at V_g = -15 V, probably due to an increased heating in the V_g = -12 V case. As expected, the efficiency at P_{1dB} is better (54%) for V_g = -15 V than for V_g = -12 V (24%).

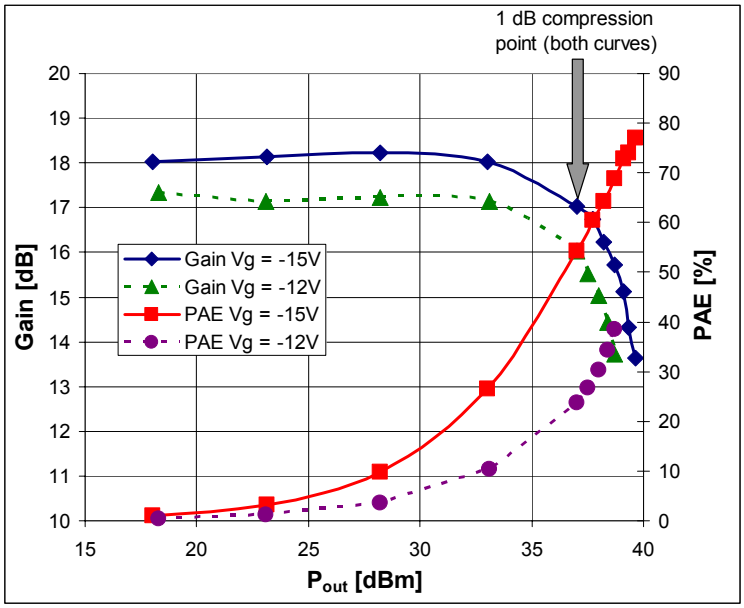

Figure 4. Measured gain and power added efficiency (PAE) at 300 MHz and V_d = 50 V as a function of output power for two different gate bias settings.

The 2:nd harmonic generation at P_{1dB} was measured to be 26 dB below the carrier at V_g = -12 V and 30 dB below the carrier at V_g = -15 V. Two tone intermodulation distortion measurements were carried out with f_1 = 295 MHz and f_2 = 305 MHz and the results can be seen in fig. 5. P_{in} and P_{out} in the figure are the sum of the power of both carrier signals. The difference in output power for the two bias settings is within the experimental error and the slope of the third order intermodulation distortion is approximately 2.8 in both cases. At P_{1dB} the IMD3 level is -24 dB and at a 10 dB back-off from P_{1dB} the IMD3 level is – 45 dB. Only the lower intermodulation product is shown in the graph, the measurement of the higher IMD3 product was ambiguous due to an inadequate source for f_2.

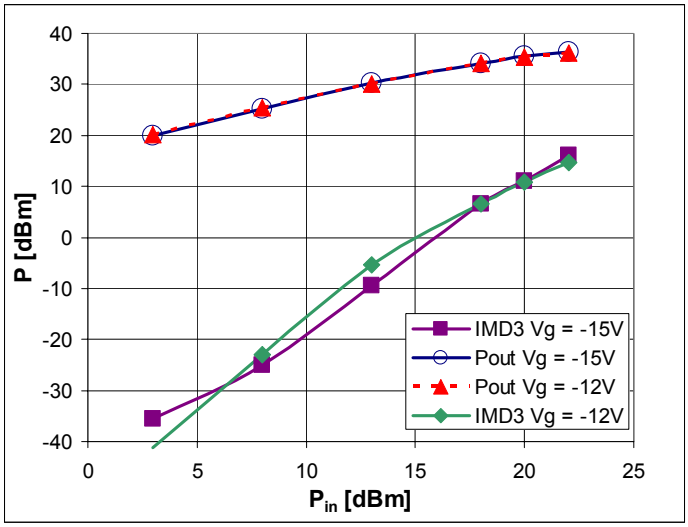

Figure 5. Two tone intermodulation properties at V_d = 50 V for two V_g settings.

CONCLUSIONS

A 100-500 MHz power amplifier was designed using a 4.6 mm gate periphery SiC MESFET. Despite the rather poor impedance matching achieved in this preliminary amplifier design we measure in the 100 – 400MHz frequency range an output power of 5 W and a gain above 13 dB at the 1 dB compression point (P_{1dB}). At 300 MHz we measured an output power of 37 dBm, a gain of 17 dB and a PAE of 54 % at P_{1dB}. The IMD3 levels at 300 MHz measured at P_{1dB} and 10 dB back-off were -24 dB and -45 dB respectively. This is a slightly better IMD behaviour than the load-pull measurements reported in [2] on a traditional SiC MESFET transistor which, however, had a much larger gate periphery. At 300 MHz the maximum measured output power and efficiency was 39.6 dBm and 77 % respectively.

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