WLAN/W-CDMA DUAL-MODE RECEIVER ARCHITECTHURE DESIGN TRADE-OFFS

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1 Introduction

This work is related to the SoCTRix-project, where a multi-standard mobile transceiver is being designed as a demonstrator. This work focuses on the two standards 802.11a and WCDMA. The mobile terminal will have a high degree of integration and a large reuse of hardware at the same time as it will support standards very different from each other. The large difference between the two considered standards put different requirements on the receiver. The main focus of this work is to find the individually best architecture for the two standards and a way to combine them with little hardware overhead.

WCDMA uses code division multiple access (CDMA). WCDMA is a spread spectrum system that spreads the data with a direct sequence (DSSS) to a chip-rate of 3.84Mcps. By using different spreading rates from 2 to 256, it can accomplish varying data-rates from 12.2kbps to almost 2Mbps. The spread data is modulated with QPSK. Different users residing on the same frequency at the same time, are separated by different orthogonal codes. Duplex is accomplished by frequency division (FDD) where transmission and reception take place simultaneously at different frequencies. For details about WCDMA see [4].

802.11a uses an orthogonal frequency division multiplexing (OFDM)transmission scheme. It can be seen as information divided between a set of sub-carriers separated in frequency. The total bandwidth used is 16.6MHz. The information is modulated on to the sub-carriers with different schemes depending on the used data-rate. For the lowest rate the modulation scheme is QPSK ranging up to 64QAM for the highest data rate of 54Mbps. In 802.11a duplex is accomplished by time division (TDD) where transmission and reception takes place at different times at the same frequency. For details about 802.11a see [5].

2 Architectures

The SoCTRix multi-standard receiver is targeting a high level of integration, which have, according to the usual arguments, ruled out a lot of known architectures. The super heterodyne need IF-filters at a relatively high frequency (compared to baseband). Both direct detection and direct sampling suffer from hitherto poor noise characteristics and low dynamic range. Sub-sampling have the same disadvantage as the direct (Nyquist) sample architecture and also put stringent requirements on the RF band-selection filter. A wide-band-IF architecture is more reasonable, but has the disadvantage of using excessive bandwidth and putting stringent requirements on the ADC-dynamic range. We are left with direct conversion and low-IF (low intermediate frequency).

Low-IF and direct conversion have common advantages and drawbacks but there are also important differences between the two. Since both architectures convert the RF-signal to very low frequency, construction of on-chip channel-select filters are simplified and the required ADC-sampling frequency is kept low. These are important aspects concerning ease of integration, power consumption and receiver flexibility. Unfortunately the low frequency of the desired signal has a couple of serious disadvantages. The 1/f-noise is large close to DC. Second order non-linearity cause intermodulation products to appear at low frequencies (DC-offset) both from self-mixing and close interferers such as in-band blockers.

3 Image Rejection

In the low-IF case an intermediate frequency is used and there is a problem with interferers at the image frequency (which in this case is the adjacent channel). These interferers may be much larger than the desired signal and put stringent constraints on image rejection. The desired signal and the image interferer are very close to each other and image rejection using RF-filters before down-conversion is not feasible. Instead other means of image rejection is needed. Using a quadrature (I/Q) representation, it is possible to distinguish between the image and the desired signal. The achievable image rejection is however limited by phase and amplitude imbalance. The

interference due to lack of image rejection is described by equation 1 [2]. P_{im} is the power present on the image frequency, γ is the magnitude of the amplitude imbalance, and ϕ is the phase imbalance in radians.

$$N_{iq} = P_{im} + 10\log\frac{1+\gamma^2+2\gamma\cos\phi}{1+\gamma^2-2\gamma\cos\phi} \quad (1)$$

The adjacent channel scenario in [4] specifies a reference signal level of $-103dBm$ together with an adjacent channel interferer of $-52dBm$. The SNR needed for demodulation of a QPSK-signal with the required $BER < 10^-3$ is roughly $7dB$, since the BER is very close to $erfc(\sqrt{E_b/N_0})$ [6]. With the spreading gain of $25dB$ associated with the specified data rate of $12.4kbps$ we can calculate the total allowed noise and distortion to be $-103-7+25 = -85dBm$. In the noise partitioning the dominant sources were: thermal noise from ADC and analogue parts (N_{ADC}, N_{ana}), quantisation noise (N_{dig}), residual noise after analogue and digital channel filtering (N_{res}), IM2 distortion (N_{IM2}) and reciprocal mixing (N_{rec}). Considering these sources, the image interference have to be kept to a level of approximately $-92dBm$. That give us a required image rejection of $-52-(-92) = 40dB$. Calculation with equation 1 show that a phase imbalance less than 1^o and an amplitude imbalance less than 1% is needed to achieve the required image rejection. This indicates that compensation in the digital domain is needed to achieve the required performance.

N_{dig}	N_{ADC}	N_{ana}	N_{IQ}	N_{res}	N_{IM2}	N_{rec}	N_{TOT}
-97dBm	-96dBm	-94dBm	-92dBm	-97dBm	-99dBm	-94dBm	-85dBm

Table 1: Excerpt from WCDMA noise partitioning.

In direct conversion we use a zero frequency IF and the desired signal is centred around DC. The occupied bandwidth is therefore smaller than or equal to, half that in the low-IF architecture (figure 1). Since the spectrum of the desired signal is not symmetric, we still have a need for image rejection as can be seen in figure 1. In this case however, the desired signal is it's own image, and the requirement on I/Q-balance is not as though as in the low-IF architecture where the image-signal may be much larger than the desired signal.

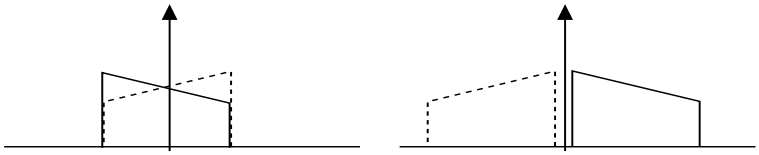


Figure 1: Spectrum of down-converted signal in low-IF and direct conversion respectively.

For 802.11a a desired signal level of -59dBm is specified for cases other then with only desired signal. For the highest order constellation diagram (64 QAM) with the need for SNR=20dB, we get a maximum level of noise and distortion $N_{TOT} = -59-20 = -79dBm$. In the noise partitioning the dominant sources of noise and distortion is: power transmitted from other channels N_{Tx}, harmonic distortion from filters and ADC N_{hd}, N_{IQ} and N_{ana}. Calculation with equation 1 calls for an I/Q-balance better than 5% and 2^o. This is not at all as hard as the requirement for WCDMA using a low-IF architecture, but still hard enough to require correction.

N_{Tx}	N_{hd}	N_{ana}	N_{IQ}	N_{TOT}
-87dBm	-89dBm	-84dBm	-85	-79dBm

Table 2: Excerpt from 802.11a noise partitioning.

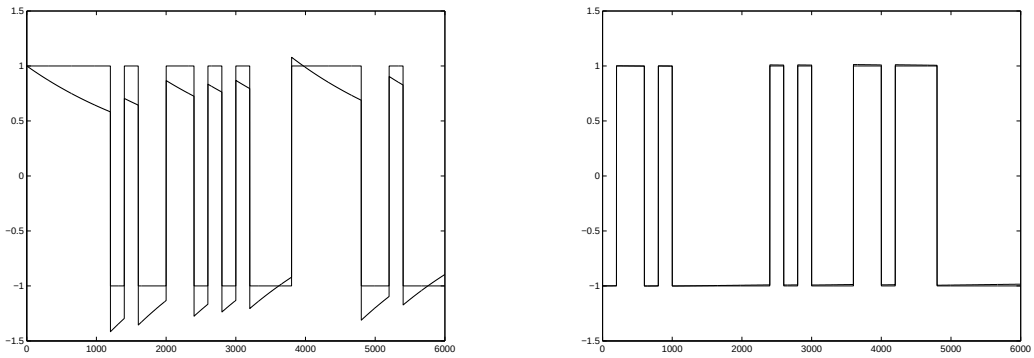
With the help from digital correction for phase and amplitude imbalance, very high levels of image rejection have been reported [3]. More than 60dB of image rejection over several MHz seems to be possible to achieve.

4 DC-offset

DC-offset problems mostly stem from self-mixing of the local oscillator, self-mixing of large interferers and from cross modulation (AM detection) from nearby large interferers such as the transmit frequency in a WCDMA transceiver. The amount of DC-offset therefore depends mainly on the amount of isolation between the LO and the mixer LO-port to places in the receiver chain before the mixer and also on the degree of second order non-linearity.

The simplest approach to solve the DC-offset problem is to use a high-pass filter preceding the low-pass channel select filter. This would get rid of a large amount of DC-offset. Unfortunately it will also affect the desired

signal when we're using direct conversion. Besides losing a very small part of the signal energy we introduce inter-symbol interference (ISI). The larger cut-off frequency we use, the larger the impact from ISI will be.



(a) (b)

Figure 2: High-pass filtered bits and their reference for (a) 50kHz cut-off frequency. Showing large ISI and (b) 1kHz cut-off frequency. ISI hardly visible.

In [4] all requirements are stated using a data rate of 12.4kbps. With a chip rate of 3.84Mcps this gives us a spreading gain of nearly 25dB. Hence the needed SNR for QPSK detection is reduced by the spreading gain to a needed SNR of roughly 7-25=-18dB. Hence we may allow the total noise and distortion to be 18dB over the desired signal. The power received is about 10dB higher than the desired signal since several users reside on the same frequency (with different codes) and therefore the total noise and distortion are allowed to be about 8dB higher than the received power. To keep the contribution from the ISI to an insignificant level, it may only be a small part of the total noise and distortion. Letting it be 10dB below the received power would fulfil that requirement. Matlab simulations indicates that a cut-off frequency of roughly 55kHz is needed for an ISI-error variance 10dB below the received signal power. See section 6.

A low cut-off frequency is associated with a long time-constant and a sudden change in DC-offset will generate an error that is slowly decaying. We get two conflicting demands on the high-pass filters cut-off frequency. We want a low cut-off frequency to avoid ISI and a high cut-off frequency to be able to recover quickly from sudden changes in DC-offset. With the help of equalisation we should be able to tolerate a larger cut-off frequency and still keep a low degree of ISI as was investigated in [1]. However, without complex equalisation or DC-offset cancellation algorithms, we have to use a low cut-off frequency and are bound by it's long time constant. With a first order high-pass filter we have the impulse response described by equation 2 and the step response is therefore described by equation 3.

$$h(t) = \delta(t) - \omega_0 e^{-\omega_0 t} \cdot u(t) \quad (2)$$

$$g(t) = e^{-\omega_0 t} \quad (3)$$

The step response tell us how long time the filter need to recover from an infinitely quick DC-offset change. If a is the level of the desired signal, b is the level of DC-offset change, the signal to DC-offset ratio (SDCR) at time t would be expressed by equation 4.

$$SDCR = \frac{a}{be^{-\omega_0 t}} \quad (4)$$

The dominating sources of DC-offset change are gain-switching of the LNA, that quickly changes the amount of LO ending up at the mixer RF-port and suddenly appearing large interferers. The first case is a little bit easier to solve since we know when and how much the gain changes. The second part is more troublesome since we can't predict when an interferer will turn up. An interferer creates a DC-offset by self-mixing due to lack of RF to LO isolation between the mixer ports. An interferer will also create a DC-offset due to second order non-linearities that will propagate to the output of the mixer due to lack of isolation between the RF-port and the mixer output. The isolation and linearity need to bee good enough to fulfil equation 4 within the desired time t.

5 1/f-noise

1/f-noise is noise which has a spectral density inversely proportional to the frequency. When the frequency is high enough, the 1/f-noise becomes insignificant and we run in to a thermal- or thermal-like noise floor. The frequency

where this approximately happens, is called the roll-off frequency. Since the noise power is inversely proportional to the frequency, the 1/f-noise energy is concentrated around DC and will affect the receiver in much the same way as a DC-offset. We are however unlikely to have quick 1/f-noise changes as we have with DC-offsets. Hence, filtering out a DC-offset also means that we get rid of a large amount of the 1/f-noise.

Compared to direct conversion, a low-IF architecture means that we have less signal energy close to DC and therefore also less 1/f-noise in our channel. Integration of the 1/f-noise spectrum over the signal bandwidth, show that the 1/f-noise inside the channel in the direct conversion case (excluding the noise within 50kHz from DC) is only about 3dB larger than in the case of low-IF where we have moved the lower part of the desired signal 100kHz away from DC. Since the total amount of 1/f-noise referred to the input only are allowed to be a small part of the thermal noise referred to the input, not to degrade the sensitivity of the receiver, the SNR improvement isn't very large.

6 Simulation

The output of the high-pass filter is a convolution of the impulse response and the input signal. The error caused by ISI would then be a convolution of the input signal and the latter part of equation 2. If we approximate the input signal with a binary sequence of -1 and 1 with the bit duration T the ISI-error at the n:th bit may be described by equation 5 in the case of a first order high-pass filter. ω_0 is the cut-off frequency in rad/s.

$$e[n] = \sum_{i=1}^{n} a_i \cdot (e^{-i\omega_0 nT} - e^{-(i-1)\omega_0 nT}) \tag{5}$$

Matlab was used to calculate the variance of the ISI-error. The error was described by 5 with the impulse response truncated to $5000 \cdot T$ and the variance was checked over 15000 bits. The simulations indicated that a cut-off frequency of approximately 55kHz was needed to achieve a signal to ISI power ratio of 10dB, which would make the ISI-error contribution insignificant.

7 Conclusions

In 802.11a the channel bandwidth is quite large and the high order constellation of 64-QAM put stringent requirements on the I/Q- phase and amplitude balance. Hence, direct conversion is very favourable here since it lessens the bandwidth as well as the requirement for I/Q-balance compared to a low-IF architecture. The problem of DC-offset cancellation in a direct conversion receiver is not so problematic to solve for 802.11a, since there is no information residing on DC. Hence, high-pass filtering is possible with no or low ISI. The conclusion is that a direct conversion architecture is the best suited for implementation of a 802.11 receiver.

In WCDMA the stringent requirement on image rejection related to a low-IF architecture presents a great drawback. The good I/Q-balance needed is however achievable with the help of digital compensation. Therefore the low-IF architecture is very attractive for a WCDMA-receiver. This is mainly because the problem with a dynamic DC-offset associated with a direct conversion solution put very stringent requirements on for example isolation between LO- and RF-paths, at the same time as it is hard to use calculations and simulations to predict exactly how tough the requirements are and if they are fulfilled.

Since the low-IF and direct conversion architectures are very much alike, they are possible to combine using the same hardware. The different requirements on the receiver components stem from the standard difference rather than from using two different but alike architectures.

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