A NON-OVERLAPPING TWO-PHASE CLOCK GENERATOR WITH ADJUSTABLE DUTY CYCLE

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ABSTRACT

In this paper, a new robust non-overlapping two-phase clock generator with adjustable duty cycle is proposed. The generator is based on a differential negative edge trigged D flip-flop and has small area and power consumption. The maximal clock rate and delay are also improved reaching a clock frequency of 1.0 GHz in a standard 0.35 µm CMOS process. The new clock generator is inherently glitch and spike free and robust against slow clock transitions, that reduces the design effort significantly.

1. INTRODUCTION

The use of the two-phase clocking scheme is motivated from a low power point of view. The combination of C^2MOS-latches, [1], and pass-transistor logic is a good candidate for low energy consumption. In order to obtain robust clocking of the C^2MOS-latches, the non-overlapping two-phase clocking scheme has to be used. A design margin for eliminating problems with clock-skew and signal-race must be included as shown in Figure 1.

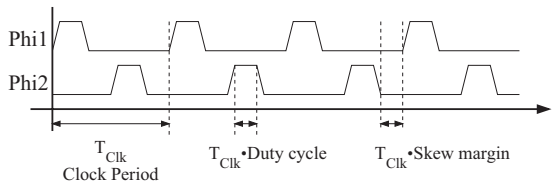

Figure 1. The non-overlapping two-phase clocking scheme

Clocking of C^2MOS-latches requires the inverse of the two clock phases *Phi*1 and *Phi*2. The inverse clocks can be locally generated by two small inverters or generated at the clock generator and globally distributed over larger areas in the chip, i.e., pseudo two-phase clocking using four clock wires. The latter scheme was used in the digital down converter chip, [2]. The clock generator presented in [3] enables another clocking strategy, i.e., distribution of a single-phase clock and use of local two-phase clock generators for each processing element. This simplifies the clock distribution network significantly, less routing, and decreased clock-skew, which enables the use of increased duty cycle.

The two-phase clocking scheme is inter alia used in mixed signal processing implemented with Switched-Capacitor circuits, SC-circuits, e.g., in sample-hold circuits. To obtain efficient clocking, the duty cycle of each clock phase should be as large as possible. This gives the charge on the capacitors time to move from one capacitor to another. However, the non-overlapping period of the clock phases must be guaranteed to avoid charge sharing between capacitors.

Hence, this calls for a non-overlapping two-phase clock generator with programmable/adjustable duty cycle.

2. CLOCK GENERATOR WITH FIXED DUTY CYCLE, BASED ON C^2MOS-LATCHES

The block diagram of the clock generator used in [2] is shown in Figure 2. The two non-overlapping clock-phases, *Phi*1 and *Phi*2, are designed from a single-phase clock ϕ, running at a double clock rate.

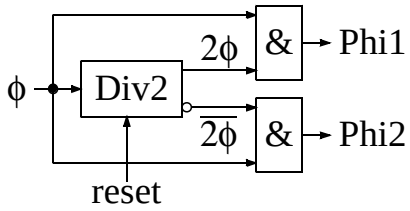

Figure 2. The two-phase clock generator

A divide-by-two circuit halves the clock rate and produces two internal clock signals, 2ϕ, and its inverse. Finally, the two clock phases *Phi*1 and *Phi*2 are obtained from two simple AND-gates, see timing diagram in Figure 3. A reset of the divide-by-two circuit is required in order to align the two phases, *Phi*1 and *Phi*2, with the main clock, ϕ. The resulting two-phase clocks have a duty cycle of 25 percent and a skew margin of 25 percent of the clock period, yielding robust two-phase clocks at an expense of speed degradation of the clocked logic due to a shorter evaluation phase. For large digital systems with high clock rates, this skew margin is motivated to obtain a robust clocking scheme. However, for analog SC-circuits this

duty cycle is too small and requires other solutions. In [2] the implementation of the divide-by-two circuit uses a standard static D-flip-flop build of C^2MOS-latches including a reset, [1], shown in Figure 4.

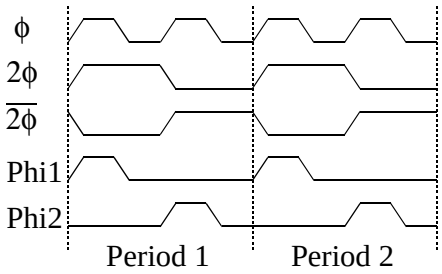

Figure 3. The timing diagram for the clock generator

Note that the inverse of the clock ϕ is required. Additionally, sharp clock slopes has to be used for correct function of the circuit. Hence, this requires large clock drivers. The divide-by- two circuit uses 28 transistors of which 8 are clocked.

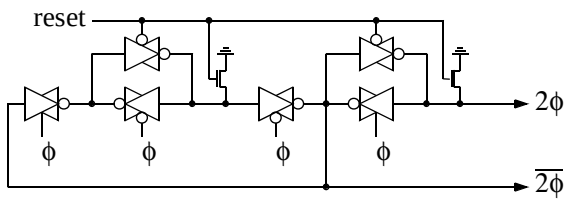

Figure 4. The divide-by-two circuit using C^2MOS-latches

In order to obtain a clock frequency of 200 MHz for the divide-by-two circuit using the AMS 5 V, 0.8 µm CMOS process, the size of the transistors had to be large. The width of the PMOS transistors was $W_P = 12\ \mu m$, which yield a large clock load. The two AND-gates were implemented with static CMOS logic style using 12 transistors. Totally, the clock generator used 40 transistors and had 8 switch nodes. The delays in the divide-by-two circuit and the AND-gates yield a large phase shift between the main clock ϕ and the outputs *Phi*1 and *Phi*2. The duty cycle of the outputs *Phi*1 and *Phi*2 was also reduced. The different delay paths in the circuit imposed a large design effort since additional delay equalization circuits were required to prevent spikes and glitches to appear the output of the clock generator. Hence, the area and power consumption increased further.

3. CLOCK GENERATOR WITH FIXED DUTY CYCLE, BASED ON A FLIP-FLOP

The basic circuit used in the non-overlapping two-phase clock generator is based on a negative edge-trigged D flip-flop designed from a DCVS-gate, [4], shown in Figure 5. The D flip-flop is a further development of the latches and the flip-flops in [5, 6] to enable merging of logic into the latches and the flip-flops. Since the master-latch is of N-type and the slave-latch is of P-type, the flip-flop becomes negative edge-trigged. The NMOS logic nets are merged with flip-flop that yielding an increased speed and lower power consumption. The flip-flop uses a similar strategy as the flip-flop in [5], the slave-latch uses a third output state during its latching phase, i.e., the output and the complementary output are allowed to go low at the same time. That flip-flop in [5] does however, suffer from the problem with charge sharing in the master-latch. With this flip-flop, these problems are eliminated. The drawback is that the clock load is somewhat increased. The flip-flop is robust against slow clock transitions, since the DCVS-gate has latched the data before the clock transitions. By replacing the cross coupled PMOS transistors with inverters, the flip-flop becomes semi-static, i.e., all nodes are fully driven during the low clock phase.

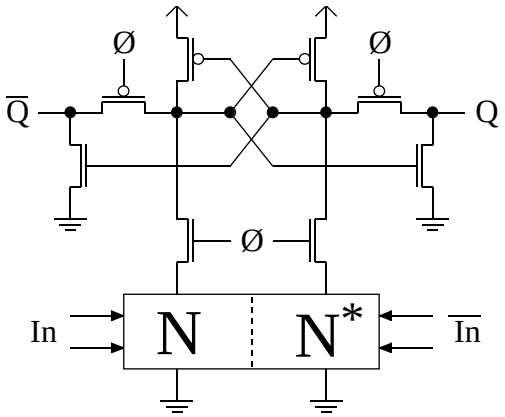

Figure 5. The negative edge trigged D flip-flop with merged NMOS logic

3.1 Design of the two-phase clock generator

The two-phase clock generator, [3], shown in Figure 6, is designed by using the D-flip-flop in Figure 5. The outputs from the D-flip-flop are fed back to the inputs accomplishing a divide-by-two circuit. A reset function is also included to make it possible to align the phase of the outputs. The circuit has two complementary outputs 2ϕ and $\overline{2\phi}$, with half the clock frequency and 50 percent duty cycle. The other two outputs *Phi*1 and *Phi*2 have the same frequency, but are phased shifted 90 degrees compared with 2ϕ, and their duty cycle is 25 percent. The circuit uses the concept of allowing the outputs *Phi*1 and *Phi*2 to go low in the latched phase. Hence, two-phase non-overlapping clocking with approximately 25 percent duty cycle is accomplished.

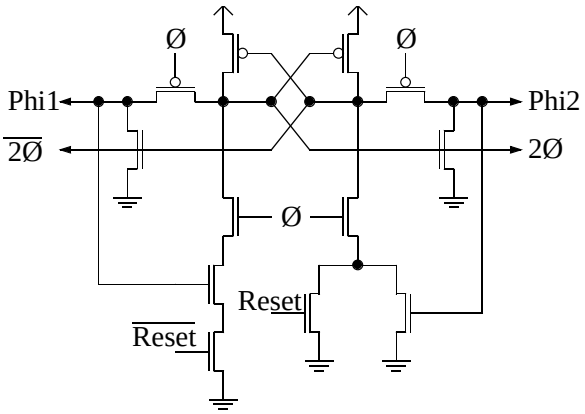

Figure 6. Non-overlapping two-phase clock generator with fixed duty cycle

The design problem, for glitch and spike free outputs, is also alleviated, since those paths with different delays does not exist. The AND-gates at the output are removed, thus the delay between the main clock and the non-overlapping clocks is minimized. The total transistor count is 12 for the dynamic and 14 for the semi-static version, respectively. The number of transistors has been reduced by 65 and 70 percent, respectively, compared with the solution in [2]. The clock load is reduced from 8 to 4 clocked transistors. The number of switched nodes is reduced from 8 to 4. Hence, the required silicon area and the power consumption are reduced.

However, comparing the area and the power consumption for the clock generator and the large clock driver is somewhat inappropriate, since the clock driver is usually much larger in both aspects. The main reasons to use this clock generator are the increased speed, ease of design, and robustness against slow clock transitions and glitches at the output of the clock generator.

4. CLOCK GENERATOR WITH PROGRAMMABLE/ADJUSTABLE DUTY CYCLE

The circuit in Figure 6 has a fixed duty cycle of approximately 25 percent. The falling edges of the outputs *Phi1* and *Phi2* are following the rising edge of the main clock ϕ, delayed by the fixed gate-delay for the clocked DCVS-gate. The duty cycle can be increased by delaying the signals to the pull-down NMOS transistors as shown in Figure 7. This yields a duty cycle corresponding equation (1). Where D is the total delay, which consists of the delay of the clocked DCVS-gate and the delay-line, and T_{Clk} is the clock period.

$$DutyCycle = 25 + \frac{D}{T_{Clk}} \cdot 100\ [\%] \qquad (1)$$

For non-overlapping clocks the duty cycle should be less than 50 percent, hence D should be held less than a quarter of the clock period. Since D is fixed the duty cycle will vary with T_{Clk}. When running the clock generator at a lower clock frequency the duty cycle decreases, yielding an increased skew margin.

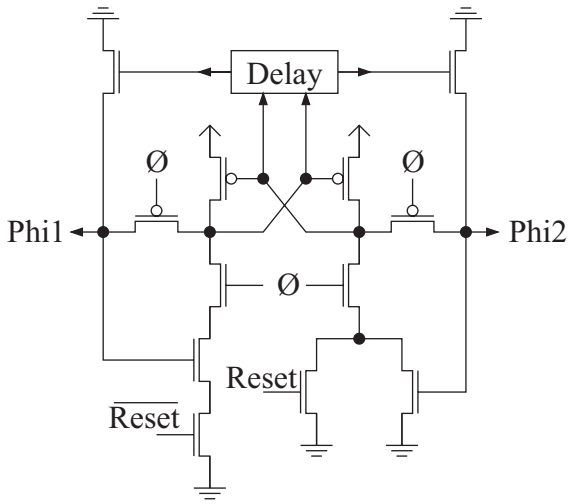

Figure 7. Two-phase clock generator with programmable/adjustable duty cycle

4.1 Implementation of the programmable fixed delay

The delay can be implemented in several ways. For a fixed delay, chains of static CMOS inverters or DCVS buffer/inverters can be used. Odd and even number of inverters can be used since the clocked DCVS-gate is differential. For a small increase of the duty cycle, the CMOS inverter chain is preferable, and for larger increase of the duty cycle, the DCVS buffer/inverter is preferable. For larger delay, an under-sized static CMOS inverter chain is also possible to use. Since only the rising-edge requires to be delayed, every other PMOS and NMOS transistor should be under-sized, except for the final PMOS transistor at the output, which should not be under-sized to get a sharp rising-edge.

4.2 Implementation of the adjustable delay

For adjustable duty cycle after fabrication of the chip, the delay could be implemented using a current controlled delay line shown in Figure 8. Only the rising edge of the output should be adjustable. Hence, only one current sink is required. In order to accomplish sharp rise and falling edges at the output, an inverter is required.

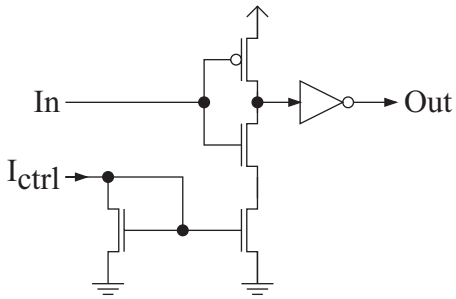

Figure 8. Current controlled delay

4.3 Simulation

All circuits are implemented in a standard 0.35 µm CMOS process and verified by simulations using HSPICE. The simulations using one and two CMOS inverters as delay are shown in Figure 9. The main clock ϕ is running at 1 GHz yielding a clock frequency for the non-overlapping clocks of 500 MHz.

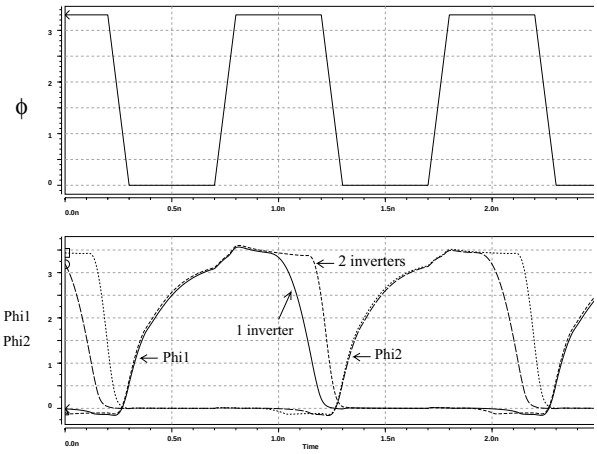

Figure 9. Simulation of the clock generator using CMOS inverter delay chains

5. CLOCK JITTER ANALYSIS

In the sampling process, the jitter of the sample clock is an important key factor. The clock generator itself does not produce any jitter, since the clock edges are following the main clock ϕ. However, variations of the power supply voltage and the bulk have to be taken into consideration. The sample instance can be defined as the time instant when the clock goes low. By designing for sharp falling edges the jitter induced by variations in the power supply voltage and bulk can be minimized. This can easily be accomplished with the novel clock generator since the NMOS transistors at the outputs are not ratio sensitive. It is also important to keep the load of the clock generator small, using buffers with minimum size inverter at the input.

6. CONCLUSION

The robust non-overlapping two-phase clock generator with adjustable duty cycle was presented. Compared with the design in [2], the new clock generator reduces the transistor count with 70 percent. The number of clocked transistors and the number of switching nodes are reduced with 50 percent. The size of the clocked transistors is also reduced. Consequently the area and power consumption are reduced. What enables a new clocking strategy with distributed clock generators controlled with a single phase clock.

Simulation in HSPICE shows that the new clock generator is faster and has lower phase shift between input and the output. A clock frequency of 1 GHz is reached using a standard 0.35 µm CMOS process. By adding delay lines, the duty cycle can be programmed/adjusted. The delays could be implemented using static CMOS inverters, DCVS buffer/inverters, or current controlled delay lines. The new clock generator is also inherently glitch- and spike free, and robust against slow clock slopes, that reduces the design effort significantly.

7. REFERENCES

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