Some aspects of modeling of dense high speed TL interconnects for printed boards

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In this paper we present some results of the ongoing research aimed at studying the limitations attached to the increase in transmission line (TL) density for the high speed interconnects at the board, multi-chip module and on-chip integration levels. For any interconnect solution the important quality in the frequency band of interest is the signal to noise ratio obtainable, where noise could be due to additional amplification required, TL itself and any cross talk signal picked up by the line.

First part of the paper deals with modeling the coupling between two TL sections in the attempt to formulate simple guidelines on how to chose the TL dimensions and adjacent trace separation to maintain reasonably low trace coupling. Second part of the paper deals with the influence of TL cross-sectional parameter upon the high frequency losses. Area efficiency parameter is introduced to allow the measure of the tradeoff between obtaining smaller loss (with wider central strips) and smaller cross talk in order to obtain the best possible throughput per board cross section at any bit error rate.

I. Coupling between adjacent TL traces

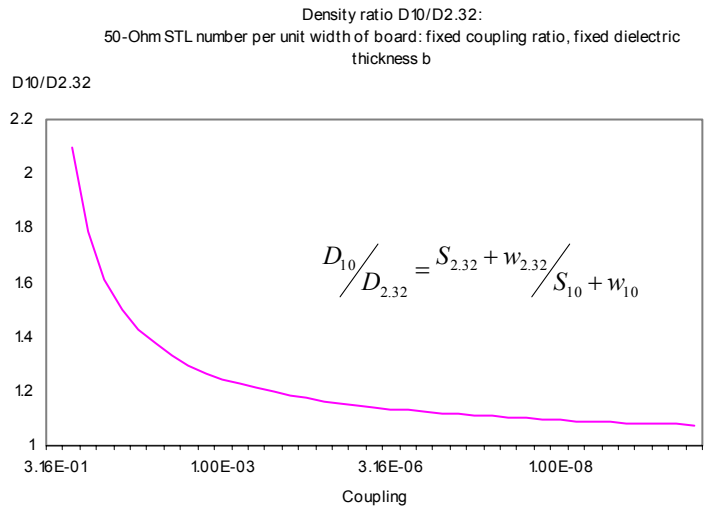
Here the main aim of study was to find a way of packing more TL traces within the same board surface still maintaining given low coupling between neighboring traces. Modeling of the parameters for edge-coupled transmission lines was carried out using quasi- analytical expressions given in the commonly known sources ([1] for the Microstrip lines, MTL and [2] for the Strip lines, STL). It should be noted here, that expressions for the coupling coefficients of the quarter- wave coupled TL sections were used. Thus corresponding values can serve only as an estimate but the qualitative conclusions can help in the design of TLs with differing length.

It appeared, that for thin TL central strip thickness does not influence coupling of adjacent traces very much, especially taking into account that we commonly use relatively low impedance lines. Strip separation and dielectric thickness play much more significant role in changing coupling coefficient.

It was also found, that changing dielectric thickness (e.g. ground- to- ground separation in STL) for the system of two adjacent lines with fixed impedance (fixed dielectric constant ε_r, fixed width- to- strip thickness ratio w/t and fixed width- to- dielectric thickness ratio w/h) will yield almost the same coupling ratio, if the separation distance is scaled correspondingly ($w/h \sim w/s$). A relatively simple rule can be used in order to maintain the adjacent 50- Ohm TL trace coupling coefficients about or below 15%: separation distance between the traces must be about or greater than twice the strip width.

It was also found, that using the dielectric material with larger dielectric constant also helps, even without changing the dielectric thickness.

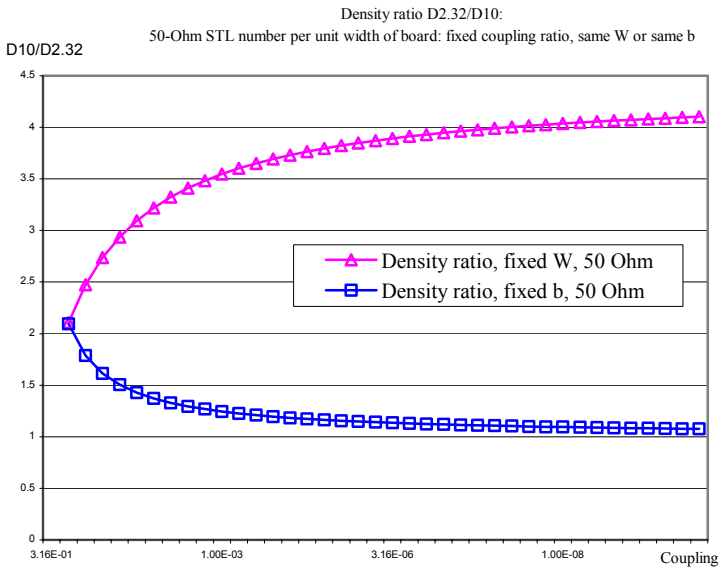
In order to find out how much better it becomes, formal "STL packing density ratio" is introduced It shows how much more STL traces per unit of board cross- sectional dimension can be put when changing substrate from FR4-like substrate (ε_r ~2.32) to the Al_2O_3- like one (ε_r ~10) still maintaining given allowed coupling ratio. Picture to the right shows the dependence of the improvement in packing density for 50-ohm copper conductor STL. It is easy to see, that for very small couplings there will be almost no gain. Level $D_{10}/D_{2.32}$ =1 corresponds to no change at all.



Of course, when moving the STL traces to another type of substrate layer as above one needs to rescale some dimensions. Another question which is relevant to ask here is: what is better, to keep the dielectric thickness and to rescale the strip width, or to keep the strip width and to rescale the dielectric thickness?

Picture to the right shows the dependences of the increase in the STL packing density for the two dielectrics (ε_r ~2.32 and ε_r ~10) while maintaining predetermined coupling between adjacent traces.
Upper line- adjusting the dielectric thickness (keeping same trace width); lower line- adjusting the trace width (keeping same dielectric thickness) to maintain same STL impedance (50 Ohm).

One can conclude, that making dielectric layer thinner and increasing the dielectric constant helps to pack more STLs into the same area without increasing coupling coefficient.



It should be noted here, that above estimations are valid for ideal dielectric substrates (no losses), when coupling coefficients are rather small and TL traces are relatively thin. But still, qualitative results should be valid for most of realistic cases.

As the discussed lines may be put within the multi-layer structures, increase in the TL packing density while tuning to thinner substrates and substrates with higher dielectric constants can be even higher, as additional layers could be introduced within allowed board thickness.

However, possible increase in TL loss at high frequencies caused by skin effect in thin TL strips with decreasing width can substantially limit the increase in the TL packing density. Thus additional studies into the current density and loss power density distributions for the TL of different geometry at high frequencies are also essential.

II. TL loss calculations

Skin effect is universally blamed for almost all bad things that happen to the high frequency signal in the conductors and TLs (losses, spectral distortions etc.). Unfortunately our knowledge of this important effect is limited. Moreover, in our existing models of skin effect very often proven facts co-exist with gross misconceptions.

In general the decrease in the signal strength at the load (with fixed power at the transmitter) at high frequencies can be caused by

i. the increase in power loss along the TL conductors (both central and current return ones);
ii. growing mismatch due to the deflection of the TL impedance from nominal (both real part from 50 ohm and imaginary part from zero).

Distortion of the signal spectrum is caused mainly by the frequency dependence of the loss and mismatch factors. Another factor is the loss in the S/N power at the load due to the increasing TL noise at high frequencies. And as it was shown above, additional problems could be brought due to the growing coupling to the neighboring traces at higher frequencies.

With the signal frequencies going into the GHz bands abovementioned problems could become pronounced even for relatively short TL sections on the printed boards, on the multi-chip modules and inside the chips themselves. Any optimization of the TL geometry should be based upon the clear understanding of the processes involved. As the correct measurements of the current density inside the tiny conductors at high frequencies are impossible, computer simulations of the current density distributions become extremely valuable [3]. Though final comparison with the experimental results is

limited to the bulk measurable parameters (like S_{11} and S_{12} for example). We present here the results of computer modeling using commercial full- 3D Maxwell equation solving simulators [4, 5] for the STL with varying central strip dimensions. Table I below gives the corresponding STL dimensions.

Table I

	L, μm	w, μm	t, μm	X, μm	Y, μm	ε	2Zo, 0.1GHz	2Zo, 20GHz
STL N0	750	50	5	50	7.5	1	50.5	53.1
STL N1	750	25	5	50	7.5	2.3	50.5	53.1
STL N2	750	15	5	50	7.5	8.4	50.4	53.1
STL N3	750	8	5	50	7.5	11	51	44.5
STL N4	750	5	5	50	7.5	14	51.2	47.7
STL N5	750	2	5	20	7.5	17.5	52.4	57.9

Here ***L*** is the structure length, w is the overall STL central strip width, ***t*** is central strip and screen thickness, ***X*** and ***Y*** are the distances from the central strip to the screen, conductor material- copper (σ=68E6 S/m). Chosen strip- to- screen separation distance in X (strip width) direction was enough to guarantee no influence of the side- walls closing the structure, upon the results. Frequency simulation range was 0.01 to 10 GHz, same for all structures. Dielectric constant was adjusted to maintain approximately constant characteristic impedance as the central conductor width was varied.

The loss power density values were obtained by integrating corresponding density distribution functions (averaged through the period) in the cross- section at the middle of TL structure. A measure called area efficiency has been introduced, defined as the area of the central conductor times the loss per unit length (in arbitrary units). This measure would be constant if loss is inversely proportional to the area. Area efficiency indicates the usefulness in increasing the cross- section of the STL central strip in decreasing the loss. Simulation results are presented in Table II below.

Table II

1	2	3	4	5	6	7	8	9	10	11	12	13	14
	loss, [power / volume]	sqrt(f) exp. Loss /act. Loss	sqrt(f) exp. Loss /act. Loss	loss* area	Area efficiency rel N0	loss* periphery	Periphery efficiency rel N0	Loss ground planes	Tot. Loss line & groundpl.	Tot. Loss * area	Area efficiency total loss	ADS loss dB	ADS s rel. loss Norm.
0.1GHz													
N0	1.78	**1.00**	0.31	44.5	**1.00**	19.6	**1.00**	1.57	3.35	83.8	1.00	0.127	0.71
N1	2.66	**1.00**	0.40	33.3	1.34	16.0	1.23	1.70	4.36	54.5	1.54	0.226	0.85
N2	5.16	**1.00**	0.33	38.7	1.15	20.6	0.95	2.06	7.22	54.2	1.55	0.516	1.00
N3	8.25	**1.00**	0.36	33.0	1.35	21.5	0.91	2.30	10.55	42.2	1.99	0.795	0.96
N4	12.2	**1.00**	0.33	30.5	1.46	24.4	0.80	2.42	14.62	36.6	2.29	1.19	0.98
N5	28.9	**1.00**	0.32	28.9	1.54	40.5	0.48	2.30	31.20	31.2	2.69	2.62	0.916
1GHz													
N0	1.73	3.25	**1.00**	43.3	**1.00**	19.0	**1.00**	1.15	2.88	72.1	1.00	0.23	1.33
N1	3.37	2.50	**1.00**	42.1	1.03	20.2	0.94	1.63	5.00	62.5	1.15	0.383	1.14
N2	5.36	3.04	**1.00**	40.2	1.08	21.4	0.89	1.96	7.32	54.9	1.31	0.805	1.59
N3	9.45	2.76	**1.00**	37.8	1.14	24.6	0.77	2.42	11.87	47.5	1.52	1.084	1.15
N4	12.9	2.99	**1.00**	32.3	1.34	25.8	0.74	2.30	15.20	38.0	1.90	1.441	1.12
N5	29.3	3.12	**1.00**	29.3	1.48	41.0	0.46	2.18	31.48	31.5	2.29	2.51	0.87
10GHz													
N0	3.73	4.77	1.47	93.3	**1.00**	41.0	**1.00**	2.56	6.29	157.3	1.00	0.771	2.07
N1	6.95	3.83	1.53	86.9	1.07	41.7	0.98	3.82	10.77	134.6	1.17	1.237	1.78
N2	10.8	4.78	1.57	81.0	1.15	43.2	0.95	4.72	15.52	116.4	1.35	2.486	2.32
N3	19.4	4.25	1.54	77.6	1.20	50.4	0.81	5.26	24.66	98.6	1.59	3.048	1.51
N4	23.3	5.24	1.75	58.3	1.60	46.6	0.88	5.90	29.20	73.0	2.15	3.656	1.57
N5	38.6	7.49	2.40	38.6	2.42	54.0	0.76	5.56	44.16	44.2	3.56	4.757	1.23

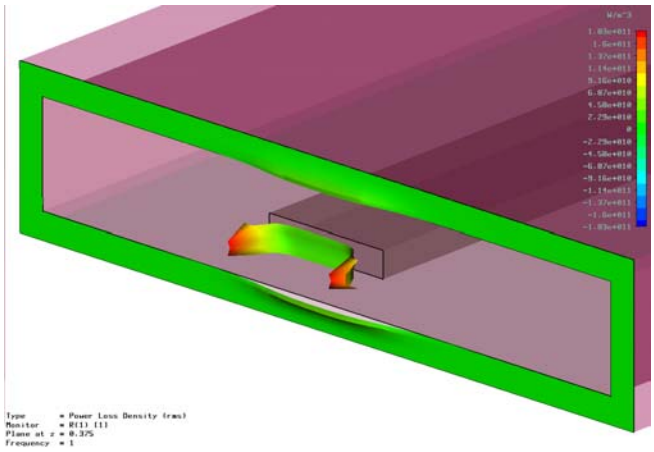
Skin depth in copper $\delta = \sqrt{2/\omega\mu\sigma}$ is 6.08, 1.92 and 0.608 μm for 0.1, 1 and 10 GHz respectively.

For very high frequencies where the skin depth is only a fraction of the conductor dimensions it is quite obvious that the loss should not scale with the inverse of area but rather by the inverse of the periphery. From the data in Table II above it is however quite apparent that "scaling with the area"

(*loss * area* =constant) relationship does not hold at all even for cases where skin depth is comparable to conductor dimensions: see column 5. It is also clear, that "scaling with the periphery" (*loss * periphery* =constant) is not accurate either: column 7.

Most probably it happens due to very uneven current distributions leading to even more uneven loss density distributions.

Figure to the right presents the "carpet" style display for the power loss density distribution for the STL N1 at 1.0 GHz (CST Simulation). Increase in the loss density at the central strip edges is clearly visible. Loss power density distributions of the "mirror currents" in lower and upper screen walls are also clear. It is also noticeable, that distribution across the strip thickness is almost uniform, as it is common for the so-called "lateral skin- effect" conditions [6].



It is usually said that from the onset of skin effect, the additional loss in the TL increases proportional to the square root of frequency. It is, though, a bit uncertain how to define this "skin-effect onset point". In some literature sources this point is defined as the frequency when the skin depth equals one half of the smallest dimension of the conductor cross- section. The data present in the Table II above show severe deviations from this simple assumption (columns 3, normalized to the 0.1 GHz case, and 4, normalized to the 1 GHz case). It is also clear that skin depth i.e. noticeable uneven current distribution onsets when the largest dimension (not the smallest) exceeds (twice) the skin depth (picture above and Table II). In the columns 13 and 14 of Table II loss values acquired using Agilent ADS [7] Line Calc simulator program are present for the comparison. Column 13 presents loss per 100 mm of copper STL with the same cross- section parameters as used in CST simulations. Column 14 is the ratio of the ADS simulated loss value divided by the CST- derived loss normalized for one particular instance (STL N2 at 0.1 GHz). It is not a comparison of actual loss values, derived by different simulators, but can only indicate to the discrepancies caused by different models of skin- effect used.

Choice of the model of the current density distribution function actually has an extreme effect upon the estimated STL loss value per unit length. Losses were calculated for the few analytical models of this distribution without skin effect and in case of well onset lateral skin effect:

$$j_z(x) = j_0;\ j_z(x) = j_0 \cdot \exp\left(\frac{a - |x|}{\delta}\right);\ j_z(x) = \frac{j_0}{\sqrt{[1-(x/a)^2]}};\ j_z(x) = \begin{cases} j_{0,} & a - \delta \le |x| \le a \\ 0, & other \end{cases}$$

Values of TL loss per unit length derived by integration of square of current density were differing up to 4 times, though normalization was used to guarantee the same overall current in the conductor.

References:

1. *"RF and Microwave Coupled Circuits",* R. Mongia, I. Bahl, P. Bhartia, Artech House, 1999, chapter 3.4.2;
2. *"Transmission Line Design Handbook"*, B. C. Wadell, Artech House, 1991, chapter 4.6.5.
3. "Microwave Circuit Modeling Using Electromagnetic Field Simulation", D.G. Swanson Jr., J. R. Hoefer, Artech House, 2003.
4. *"CST Microwave Studio",* Computer Simulation Technologies, http://www.cst.de/index.htm?page=/products/mws/mws.htm
5. *HFSS- High Frequency Simulation Software* by Ansoft , http://www.ansoft.com/products/hf/hfss/
6. "Lateral skin Effect in a Flat Conductor", V. Belevich, http://www.cvni.net/abc/rip2/r9/r0901.html
7. *ADS- Advanced Design System, Agilent,* http://eesof.tm.agilent.com/products/adsoview.html