

DESIGN OF A PULSED, 10 W, Ku-BAND SOLID-STATE AMPLIFIER FOR RADAR TRANSMITTERS

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SUMMARY

In radar applications there is a need for high power amplifiers. This paper describes the design and performance of a pulsed solid state amplifier for radar transmitters. The amplifier is designed of four cascaded commercial amplifiers (Excelics 8 W Internally Matched Power FET, EIA 1616-8P) with micro strip technology on Rogers laminate RO3000. The amplifier works in frequency range 15.5 to 17.5 GHz. The drain voltage is pulsed by a pulse aggregate also designed at Saab Bofors Dynamics. In pulse mode the output power is 10 W (40 dBm) in the frequency range 15.5 to 16.5 GHz and the gain is about 20 dB. In this paper we describe the amplifier design and performance. We also show the results from simulations and measurements during the design stage and discuss the problems we had.

INTRODUCTION

A solid-state amplifier for radar applications in Ku-band has been designed. Figure 1 shows a picture of the amplifier.

The figure shows a picture of the box where the microwave circuits and the pulse aggregate is placed. The box is made of brass and the outer size of the box is 130 mm x 50 mm x 35 mm, L (without connections) x W x H respectively. The connections is of type sma for the RF in and RF out. The pins for voltage feeding are pins with Pi circuit filters. The box length with connections is 150 mm.



Figure 1 Picture of the amplifier.

The amplifier works in the frequency range 15,5 GHz to 17,5 GHz. The transistors used are specified in the frequency range 16,2 GHz to 16,4 GHz. Thus in this application they are used outside there specified range. The transistors used are Excelics 8 W Internally Matched Power FET, EIA 1616-8P. They are specified to have an output power of typical 39 dBm (7,9 W) and minimum 38 dBm (6,3 W) in the range 16,2 GHz to 16,4 GHz. In this application we use a pulse aggregate to instantaneous get higher output power. In the frequency range 15,5 GHz to 16,5 GHz the output power is 40 dBm (10 W) with input power 23 dBm and in the range 16,5 GHz to 17,5 GHz the power gradually decrease to 37 dBm (5 W). The reason for this decrease in output power will be discussed later in the design section. Figure 2 shows the amplifiers output power and gain when the input power is 23 dBm.

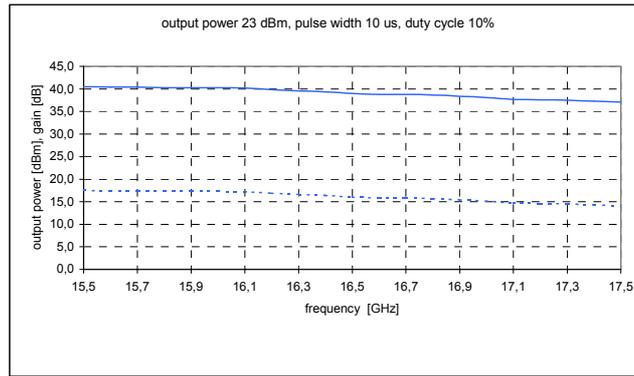


Figure 2 The amplifiers output power and gain with input power 23 dBm, pulse width 10 μ s and duty cycle 10 %.

DESCRIPTION OF THE AMPLIFIER

The pulse aggregate and the microwave circuits are placed on opposite sides in the box. The pulse aggregate card is shown in figure 3 and the microwave circuit card in figure 4.

Pulse aggregate

The pulse aggregate is designed at Saab Bofors Dynamics. It is designed to handle a pulse width of maximum 50 μ s and a duty cycle of less than 30% is recommended. The aggregate is protected from incorrect voltage feed. The pulse input at the card is AC-coupled in a way that the outputs are turned off if the input signal is high more than 1 ms. The delay between the card input and output is 200 ns. Distributed so that 100 ns is delay time and 100 ns is rise- and fall time.

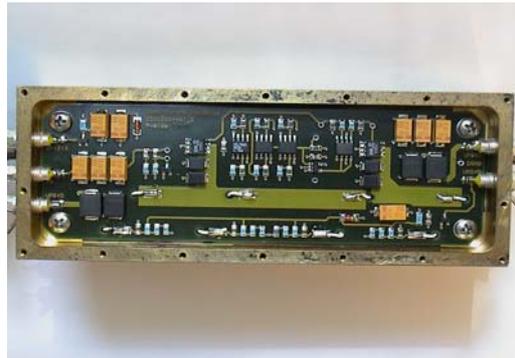


Figure 3 Picture of the pulse aggregate electronics card.

Microwave circuits

The microwave circuit of the amplifier is build of four modules, see figure 4. Between module 2 and 3 a high pass filter was placed to protect the amplifier from self-oscillation. The biasing circuits are designed with band exclusion filters to prevent self-oscillation.



Figure 4 The amplifiers microwave circuits.

DESIGN

The microwave circuits were designed in Agilent's simulation program ADS (Advance Design System). In the first design we had a problem with self-oscillation and therefore we redesigned the biasing circuits. Figure 5 shows the results from measurements and simulations of the circuit of one module where the transistor has been replaced with a microstrip line. The measurements and simulations are made between the RF input to the module and the RF output from the module.

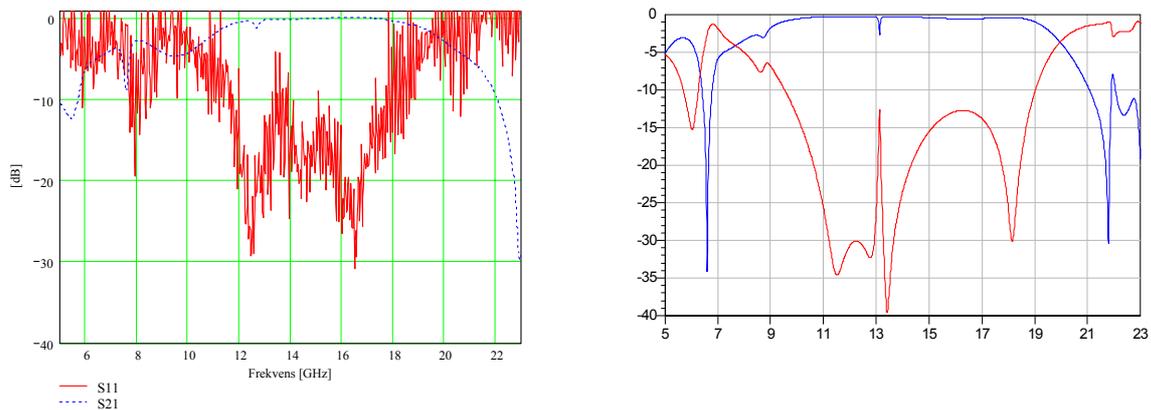


Figure 5 The left diagram shows the result from measurement and the right from simulations of the biasing circuits in figure 4.

The amplifier operates in the frequency range 15,5 GHz to 17,5 GHz. The goal was to reach an output power of 40 dBm (10 W) in the frequency range. Investigation of a single transistor indicated that it was possible to reach the goal with a pulsed signal and at 3 dB compression point. With gate and drain voltage chosen to $-0,5$ V and 9 V respectively. Figure 6 shows the result from measurement on a single sample with pulse width 40 μ s and duty cycle 1%.

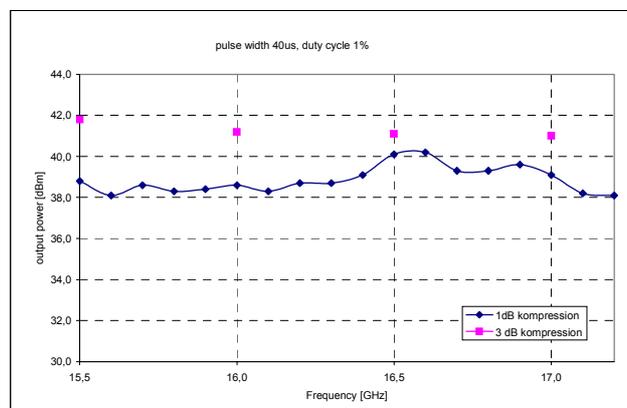


Figure 6 Output power from a single transistor.

The drain voltage at the last module was chosen to 9 V to get as much output power as possible. There is a risk that the transistor in the third module can deliver too much power to the last transistor and damage it. For that reason the drain voltage for transistor one to three were chosen to 6 V. The last FET is biased with a direct current of three to four ampere momentary. The width of the microstrip line of the band exclusion filter is typical tenths of millimetres. An investigation if the conductors could withstand the high drain current was made. The result shows that a microstrip line, with width 0.17 mm, can withstand a DC current of 4 Ampere for more than one hour^[1].

As seen in figure 2 we did not reach the goal 40 dBm output power in frequency range 15,5 GHz to 17,5 GHz. An investigation was done to figure out the reason to the decrease in output power between 16,2 GHz and 17 GHz. The fourth transistor was replaced by a conductor and the output power from the third part was measured. The result showed that the third transistor was saturated before the fourth transistor was in compression. Figure 7 shows the output power as a function of input power for frequencies between 16 GHz and 17 GHz.

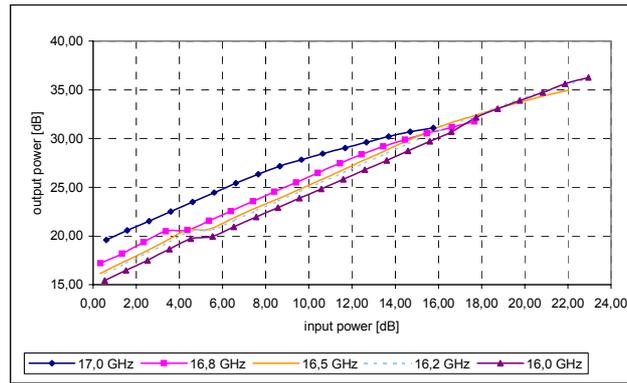


Figure 7 Output power at five frequencies between 16 GHz and 17 GHz.

At 17 GHz the transistor is saturated with the input power 16 dBm. By using a higher drain voltage the saturation point could be higher but in that case there is a risk that the fourth transistor gets too much power at the input. Nowadays Excelics manufacture 4 W transistors as well as 8 W. At the time when the amplifier was designed there were no 4 W transistors available. That is the reason why we used 8 W transistors in all four stages.

CONCLUSION

A pulsed solid state 10 W amplifier for radar transmitters has been designed. The amplifier works in frequency range 15.5 to 17.5 GHz. The drain voltage is pulsed by a pulse aggregate. In pulse mode the output power is 10 W (40 dBm) in the frequency range 15.5 to 16.5 GHz, in the range 16.5 GHz to 17.5 GHz the power gradually decrease to 37 dBm (5 W). The small signal gain is about 20 dB. By using 4 W transistors in stage one to for we think it is possible to get an output power of 10 W in the frequency range 15.5 to 17.5 GHz. By parallel couple transistors in the last stage we think that more output power can be reached.

REFERENCES

[1] A-M Andersson, C-G Svensson, "Temperature rise, due to high DC currents, in bias circuits of microstrip lines", GHz 2001.