RECENT RESULTS FROM SiC RESEARCH PROJECT AT THALES : EFFECT OF PASSIVATION ON DEVICE STABILITY AND GATE REVERSE CHARACTERISTICS ON 4H-SIC MESFETS

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Abstract. Several passivation schemes on 4H-SiC MESFETs have been studied. Two main configurations are compared. MESFET structures with thin passivation layer or no passivation layer (Configuration 1) exhibit high breakdown voltage but also current instability after high voltage Vds stress. Thick SiO_2 passivation covering the gate (Configuration 2) improves the current stability but yields lower breakdown voltage and higher gate leakage current. Surface trapping effects are considered as the main cause of the observed phenomena.

Introduction

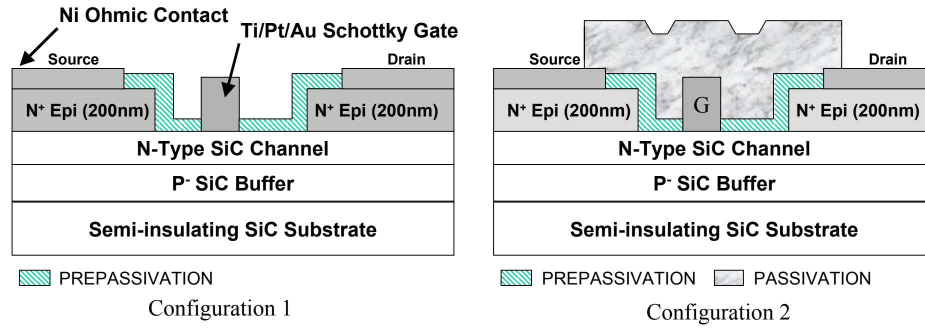
Transistors based on wide band gap semiconductors have been studied for about 10 years for RF and microwave power amplifiers. Today, the most promising prototype structures, such as III-N HEMT [1], SiC SITs and SiC MESFETs [2], provide good RF power performance, paving the way to industrial applications such as base station, or radar transmitters [3]. Still, the reliability of these new devices remains a weak point on the way towards industrialization. One key concern resides in the fact that, today, the same insulator materials optimized for the previous silicon and GaAs technologies are used for passivating the new wide band gap devices, although they are submitted to electric field five to ten-fold higher. Another key issue is related to the wide band gap semiconductor surface or interface with insulators. This surface exhibits large density of surface states, inducing charge trapping effects related to carrier injection [4,5]. Surface charges can have electrostatic influence on the device channel, and may induce DC and / or RF-dispersion, together with limitation of RF power performance. Recently, surface states instabilities as well as the effects of passivation on III-N HEMT devices characteristics, have received an increasing attention [6, 7]. On the other hand, only limited literature is available so far on surface effects in SiC MESFET [8,9].

In this paper, we report on the effect of the passivation on the stability of SiC MESFET characteristics. Two main variants have been studied and compared. First, MESFET with no passivation or a thin insulator (<50nm) (Configuration.1), and secondly, MESFET with a thick passivation (>200nm) covering the device (Configuration. 2). Devices in Config.1 will generally exhibit high breakdown voltage but unstable DC characteristics. In contrast, a device in Config.2 will generally exhibit high stability but lower breakdown voltage.

Device structure and processing

HTCVD Semi Insulating substrates were mainly supplied by OKMETIC except one HPSI substrate from CREE Research. The epitaxy, supplied by OKMETIC on all wafers, includes a P-type buffer layer (Na $\approx$1-3 $x10^{17}$ cm^{-3}), a N-type active layer (Nd =1-3$x10^{17}$ cm^{-3}) and a N+ contact layer (Nd >1$x10^{19}$ cm^{-3}). Standard process consists in MESA isolation by RIE etch and a 250nm deep recess, also RIE etched, to define the channel in the active layer. In order to protect the active layer, and prior to ohmic contact metal deposition, 50nm thick insulator is either grown by 6 hours wet oxidation (resulting in SiO_2), or deposited using PECVD (SiO_2 or Si_3N_4). We call this thin insulating layer “prepassivation”. Then, ohmic contacts are made, consisting of 100nm Ni based metallisation e-beam evaporated after self-aligned RIE etch of the prepassivation thin layer, and metal lift-off. After annealing (950°; 5min), good

morphology and electrical characteristics of the ohmic contact are reproducibly achieved (Ra~2nm, $\rho_c=2x10^{-6}$ $\Omega.cm^2$). The same kind of lift-off process is used to deposit the multi-layer gate Ti(50nm) Pt(50nm) Au(500nm) with 2.5µm Lgd spacing. At this stage, the transistor is completed and can be measured (Config.1). Then, thick passivation is deposited, either mineral SiO_2 or Si_3N_4 layer using PECVD, or BCB polymer from Dow Chemicals deposited by spin-on technique and annealed [10]. At this stage, the device has reached its final state (Config. 2, see figure 1). Table 1 summarises the different combinations studied for "prepassivation" and "passivation" layers



Configuration 1 Configuration 2

Fig 1: Main passivation schemes: config.1 (thin mineral protection or free SiC surface), and config.2 (thick passivation covering the gate).

Table 1: Prepassivation and passivation combinations explored in this study. Also indicated, the breakdown voltage measured before and after thick passivation. "WO " indicates the presence of a "walk out" phenomenon:

Sample	*Substrate*	*Prepassivation (50nm)*	*BVgd1*	*Passivation*	*BVgd2*
X_59	HTCVD (OKM)	Thermal Oxide	>250V	PECVD SiO_2/ Si_3N_4 (400/50nm)	80-180
X_84	HTCVD (OKM)	Thermal Oxide	>250V	PECVD SiO_2/ Si_3N_4 (400/50nm)	110
X_85	HTCVD (OKM)	Thermal Oxide	>250V	PECVD SiO_2/ Si_3N_4 (400/50nm)	140
X_60	HTCVD (OKM)	PECVD Oxide	>250V	PECVD SiO_2/ Si_3N_4 (400/50nm)	200
X_62	HTCVD (OKM)	PECVD Oxide	>250V	No	-
X_82	HTCVD (OKM)	PECVD Si_3N_4	>250V	PECVD Si_3N_4 (200nm)	120 (WO)
X_83	HTCVD (OKM)	PECVD Si_3N_4	>250V	PECVD SiO_2/ Si_3N_4 (400/50nm)	190 (WO)
X_86	HPSI (CREE)	PECVD Si_3N_4	200V	PECVD SiO_2/ Si_3N_4 (400/50nm)	150 (WO)
X_61	HTCVD (OKM)	No	>250V	BCB	180 (WO)

Measurements and experimental results

Current stability for Vds < 40V

In Config. 1, whatever the nature of the prepassivation layer, and even in the absence of any prepassivation layer (sample X_61), the following behavior is observed : the DC characteristics are highly unstable after high Vds stress, resulting in a quasi-instantaneous collapse of the drain current during the 50 Hz sweeping measurements when increasing the gate voltage stepping from zero to pinch-off voltage. Also, there is a slow recovery (seconds to minutes) after drain voltage stress under pinch off conditions (keeping Vds < 40V). In Config. 2, the thick passivation layer covering the device dramatically improves its stability. Only a slow transient may be observed, with a drain current decrease by less than 5% during the device turn-on, or after stress.

Fig. 2a and 2b show the characteristics of a transistor before and after 2min stress (Vgs = Vpinch off, Vds = 20V) for the two configurations. Fig. 2c shows the drain current recovery after stress. On devices with thin passivation, the recovery is very slow (>10s). This relaxation cannot be described with one time-constant.

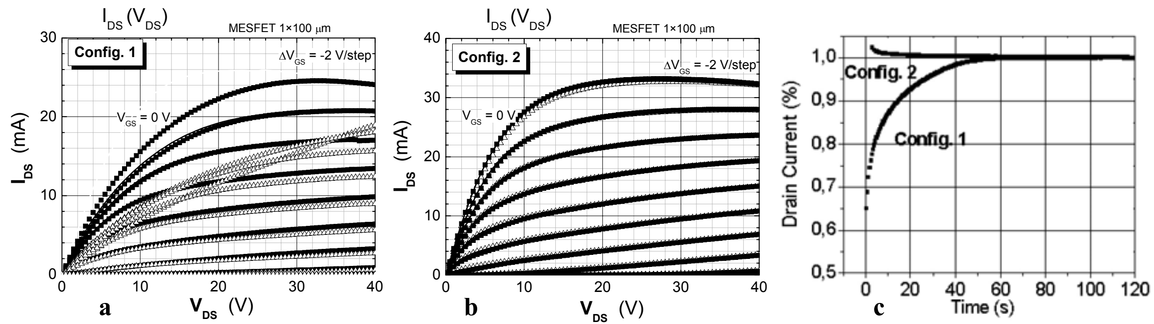


Figure 2: Drain current before (full square) and after (open triangle) 2min stress under pinch-off conditions (Vds=20V) for Config. 1 (Fig.2a) and Config. 2 (Fig.2b). Slow drain current relaxation after stress (Figure 2c).

Breakdown Voltage, Gate Leakage Current, Stability at High Voltage (Vds > 40V)

Gate to drain junction breakdown voltage (BVgd) was defined at a gate leakage current of 1mA/mm with floating source. Usually, breakdown of the MESFET is observed by further increasing the voltage by 10 to 20V. Gate to Drain leakage and breakdown voltage were measured before and after thick passivation. On all wafers, the same trend is observed :

A dramatic increase of the gate leakage current for Vds>40V is measured after full passivation (see fig.3), while no significant difference of leakage is observed for Vds<40V. The degradation in leakage current happens together with a decrease in breakdown voltage. Before passivation, BVgd is usually >250V for all prepassivation configurations (see table 1), whereas, after thick passivation, the breakdown voltage dramatically decrease to typically 80 – 140 V, seldom 240V, mainly depending on active layer epitaxy characteristics. Etching of the thick passivation leads back to the initial state : current instability and higher breakdown voltage.

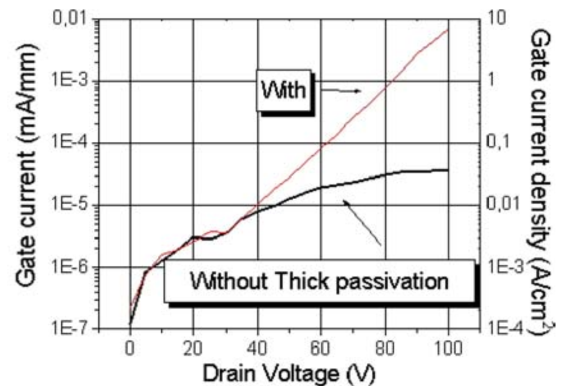


Fig. 3: Gate leakage current increase after thick passivation deposition

Discussion

Without passivation or with thin passivation (50nm), our recess 4H-SiC MESFETs presents large current instabilities attributed to surface electron trapping on prepassivation surface or at the SiC free surface near the drain side of the gate edge. The parasitic depletion caused by the trapping of electrons brings an increase of the breakdown voltage, but lowers the drain current, In this configuration, RF power measurements yield low RF power density (typically < 1W/mm).

Any thick (> 200 nm) passivation layer, covering the gate, suppresses drain current instability, at least for low voltage Vdg (<40V), but decreases the breakdown voltage. Similar conclusions can be found in recent literature [11]. Despite this degradation, RF measurement results on these stable devices are generally good, even on transistors with large periphery (up to 30 mm). At high voltage, near breakdown, injection of electrons in the insulator or at the interface may occur, depending on the passivation scheme. This injection reduces the field crowding on the gate edge and leads to the observed “walk out “ phenomena illustrated by a drift to a higher value of the breakdown when pushing the drain voltage [12] (see table 1).

We find that silicon nitride, or at least the PECVD silicon nitride used in our study is not suitable for long term reliability or stability of the device, probably due to easier electron injection into the insulator, as compared to silicon oxide [13]. BCB alone brings the same kind of limitations. Using silicon oxide for both passivation and prepassivation layers provides better stability at high voltage, although SiO_2 is not free from carrier injection [4], which may result into long term reliability problems. Today, we do not have enough information to detect any difference between oxides either PECVD deposited or grown by wet oxidation. By trying different PECVD oxides, we have been able to test the influence of the quality of the oxide on the device performance. We find that oxide quality (fixed charges, interfaces states, breakdown strength) plays a key role both close to the SiC surface (prepassivation) and in the upper layer (passivation).

Surface preparation may also be important, although it requires a very large effort to get reliable conclusions. Our lift off process restricts the choice for surface treatment. At last, since the best possible insulators have to be used, alternative insulators may also be tried such as those with high dielectric constant, like HfO_2 [5]. Another way to improve stability and reliability of SiC devices, such as MESFETs, is to reduce the high field near the drain side of the gate. Like for any high voltage device, gate peripheral protection using field plates, buried gate [14], floating additional gates, JTE, resurf, p-type or undoped cap layers, . . . can increase the breakdown voltage and limit carrier injection, but they are difficult to fabricate.

Conclusion

In this study, even if we cannot completely exclude substrate trapping issues, they seem to be no longer the main limiting problems for further improvement of SiC MESFET performance when using high purity substrates [15,16]. We find good quality thick mineral passivation to be essential to provide stable DC and RF characteristics. Therefore, improvement of insulator and its interface with SiC is a key issue for future industrialization of SiC devices for RF and microwave power amplifiers.

It should be stressed that other wide bandgap semiconductors devices such as AlGaN/GaN HEMT, also working within the same high field range, present very similar problems as those we have discussed for SiC MESFET [7,17]. In particular, hot electron stress degradation on AlGaN/GaN HEMT passivated with silicon nitride have been recently observed [17].

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